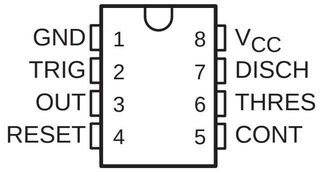
NE555, NE555Y, SA555, SE555, SE555C
PRECISION TIMERS

SLFS022A – SEPTEMBER 1973 – REVISED SEPTEMBER 2000

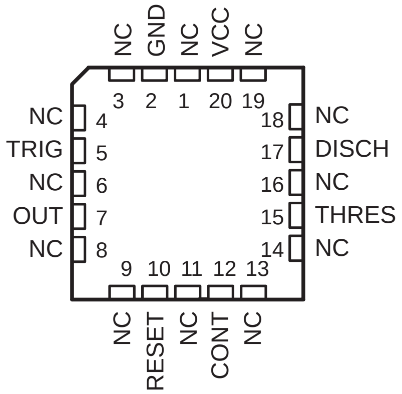
- **Timing From Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source up to 200 mA**
- **Designed To Be Interchangeable With Signetics NE555, SA555, SE555, and SE555C**

SE555C FROM TI IS NOT RECOMMENDED FOR NEW DESIGNS

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

These devices are precision monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. RESET can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between DISCH and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

The NE555 is characterized for operation from 0°C to 70°C. The SA555 is characterized for operation from –40°C to 85°C. The SE555 and SE555C are characterized for operation over the full military range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE					CHIP FORM (Y)
	V_{THRES} MAX V_{CC} = 15 V	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	11.2 V	NE555D			NE555P	NE555Y
–40°C to 85°C	11.2 V	SA555D			SA555P	
–55°C to 125°C	10.6 V 11.2 V	SE555D SE555CD	SE555FK SE555CFK	SE555JG SE555CJG	SE555P SE555CP	

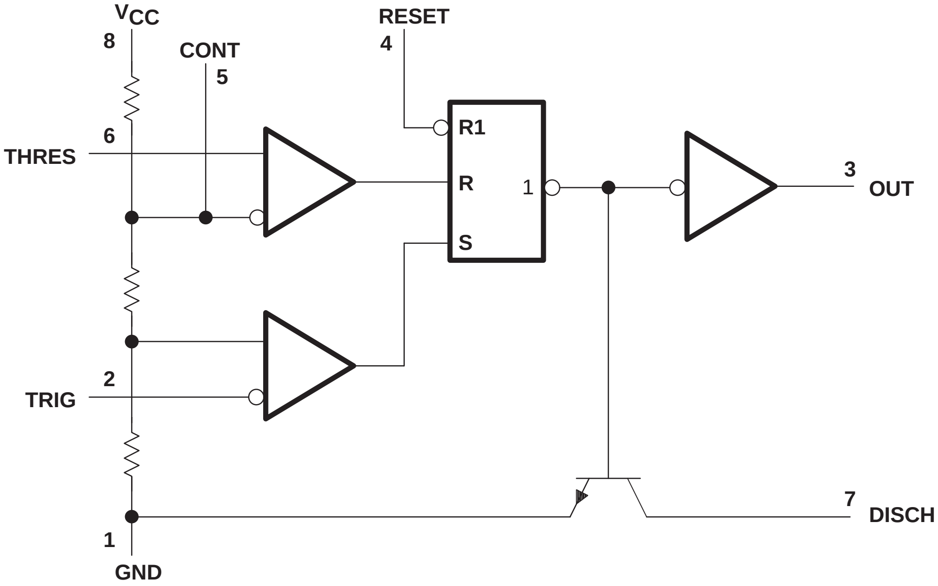
The D package also is available taped and reeled. Add the suffix R to the device type (e.g., NE555DR).

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{DD}	Irrelevant	High	Off
High	>1/3 V_{DD}	>2/3 V_{DD}	Low	On
High	>1/3 V_{DD}	<2/3 V_{DD}	As previously established	

† Voltage levels shown are nominal.

functional block diagram



RESET can override TRIG, which can override THRES.
Pin numbers shown are for the D, JG, and P packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	18 V
Input voltage (CONT, RESET, THRES, and TRIG)	V_{CC}
Output current	±225 mA
Continuous total dissipation	See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 2): D package	97°C/W
P package	85°C/W
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Storage temperature range, T_{stg}	–65°C to 150°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (SE555, SE555C)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (SA555, NE555C)	825 mW	6.6 mW/°C	528 mW	429 mW	N/A

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}	SA555, SE555C, NE555	4.5	16	V
	SE555	4.5	18	
Input voltage (CONT, RESET, THRES, and TRIG)			V_{CC}	V
Output current			±200	mA
Operating free-air temperature, T_A	NE555	0	70	°C
	SA555	–40	85	
	SE555, SE555C	–55	125	

electrical characteristics, V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			NE555 SA555 SE555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THRES voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
THRES current (see Note 3)				30	250		30	250	nA
TRIG voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
		T_A = –55°C to 125°C	3		6				
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
		T_A = –55°C to 125°C			1.9				
TRIG current	TRIG at 0 V			0.5	0.9		0.5	2	µA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
	T_A = –55°C to 125°C				1.1				
RESET current	RESET at V_{CC}			0.1	0.4		0.1	0.4	mA
	RESET at 0 V			–0.4	–1		–0.4	–1.5	
DISCH switch off-state current				20	100		20	100	nA
CONT voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
		T_A = –55°C to 125°C	9.6		10.4				
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
		T_A = –55°C to 125°C	2.9		3.8				
Low-level output voltage	V_{CC} = 15 V, I_{OL} = 10 mA			0.1	0.15		0.1	0.25	V
		T_A = –55°C to 125°C			0.2				
	V_{CC} = 15 V, I_{OL} = 50 mA			0.4	0.5		0.4	0.75	
		T_A = –55°C to 125°C			1				
	V_{CC} = 15 V, I_{OL} = 100 mA			2	2.2		2	2.5	
		T_A = –55°C to 125°C			2.7				
	V_{CC} = 15 V,	I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V, I_{OL} = 3.5 mA	T_A = –55°C to 125°C			0.35				
	V_{CC} = 5 V, I_{OL} = 5 mA			0.1	0.2		0.1	0.35	
		T_A = –55°C to 125°C			0.8				
	V_{CC} = 5 V,	I_{OL} = 8 mA		0.15	0.25		0.15	0.4	
High-level output voltage	V_{CC} = 15 V, I_{OH} = –100 mA		13	13.3		12.75	13.3		V
		T_A = –55°C to 125°C	12						
	V_{CC} = 15 V,	I_{OH} = –200 mA		12.5			12.5		
	V_{CC} = 5 V, I_{OH} = –100 mA		3	3.3		2.75	3.3		
		T_A = –55°C to 125°C	2						
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	10		9	13	
		V_{CC} = 5 V		2	4		2	5	

NOTE 3: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is $R = R_A + R_B \approx 3.4\ M\Omega$, and for V_{CC} = 15 V, the maximum value is 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS[†]	SE555			NE555 SA555 SE555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval[‡]	Each timer, monostable[§]	T_A = 25°C		0.5%	1.5%*		1%	3%	
	Each timer, astable[¶]			1.5%			2.25%		
Temperature coefficient of timing interval	Each timer, monostable[§]	T_A = MIN to MAX		30	100*		50		ppm/°C
	Each timer, astable[¶]			90			150		
Supply-voltage sensitivity of timing interval	Each timer, monostable[§]	T_A = 25°C		0.05	0.2*		0.1	0.5	%/V
	Each timer, astable[¶]			0.15			0.3		
Output-pulse rise time		C_L = 15 pF, T_A = 25°C		100	200*		100	300	ns
Output-pulse fall time				100	200*		100	300	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

[§] Values specified are for a device in a monostable circuit similar to Figure 9, with the following component values: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.

[¶] Values specified are for a device in an astable circuit similar to Figure 12, with the following component values: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

electrical characteristics, V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		NE555Y			UNIT
			MIN	TYP	MAX	
THRES voltage level	V_{CC} = 15 V		8.8	10	11.2	V
	V_{CC} = 5 V		2.4	3.3	4.2	
THRES current (see Note 4)				30	250	nA
TRIG voltage level	V_{CC} = 15 V		4.5	5	5.6	V
	V_{CC} = 5 V		1.1	1.67	2.2	
TRIG current	TRIG at 0 V			0.5	2	μA
RESET voltage level			0.3	0.7	1	V
RESET current	RESET at V_{CC}			0.1	0.4	mA
	RESET at 0 V			–0.4	–1.5	
DISCH switch off-state current				20	100	nA
CONT voltage (open circuit)	V_{CC} = 15 V		9	10	11	V
	V_{CC} = 5 V		2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.75	
		I_{OL} = 100 mA		2	2.5	
		I_{OL} = 200 mA		2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.35	
		I_{OL} = 8 mA		0.15	0.4	
High-level output voltage	V_{CC} = 15 V	I_{OH} = –100 mA	12.75	13.3		V
		I_{OH} = –200 mA		12.5		
	V_{CC} = 5 V	I_{OH} = –100 mA	2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		10	15	mA
		V_{CC} = 5 V		3	6	
	Output high, No load	V_{CC} = 15 V		9	13	
		V_{CC} = 5 V		2	5	

NOTES: 4. This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is $R = R_A + R_B \approx 3.4\ M\Omega$, and for V_{CC} = 15 V, the maximum value is 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	NE555Y			UNIT
			MIN	TYP	MAX	
Initial error of timing interval[†]	Each timer, monostable[‡]			1%	3%	
	Each timer, astable[§]			2.25%		
Supply-voltage sensitivity of timing interval	Each timer, monostable[‡]			0.1	0.5	%/V
	Each timer, astable[§]			0.3		
Output-pulse rise time		C_L = 15 pF		100	300	ns
Output-pulse fall time				100	300	

[†] Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

[‡] Values specified are for a device in a monostable circuit similar to Figure 9, with the following component values: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.

[§] Values specified are for a device in an astable circuit similar to Figure 12, with the following component values: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

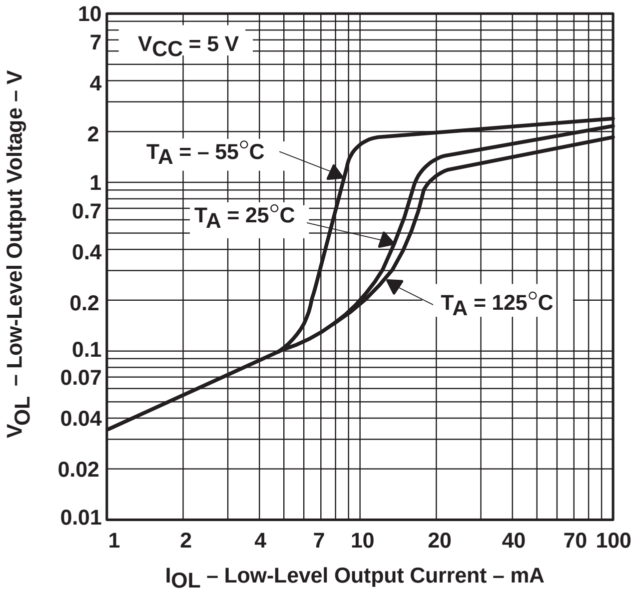


Figure 1

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

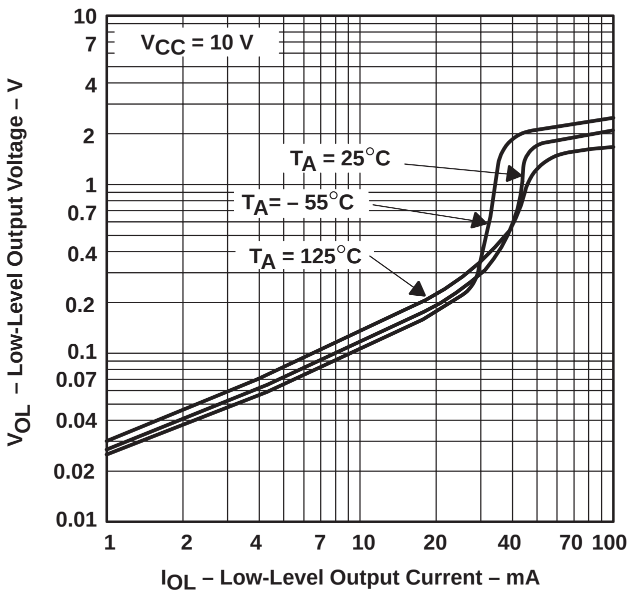


Figure 2

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

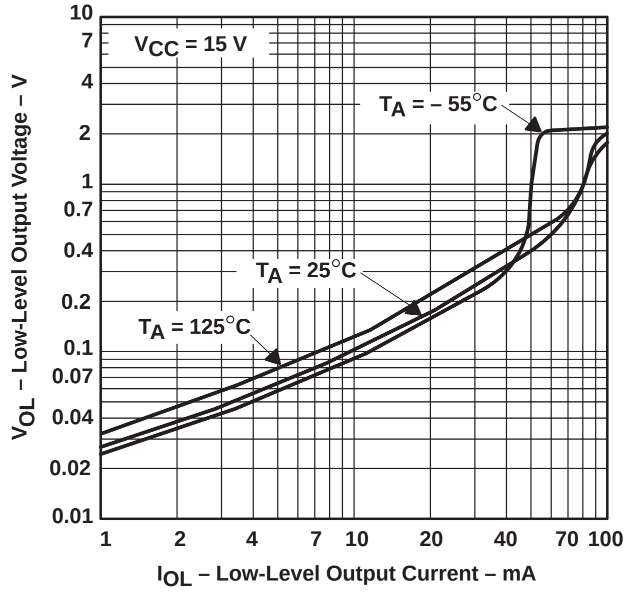


Figure 3

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT vs HIGH-LEVEL OUTPUT CURRENT

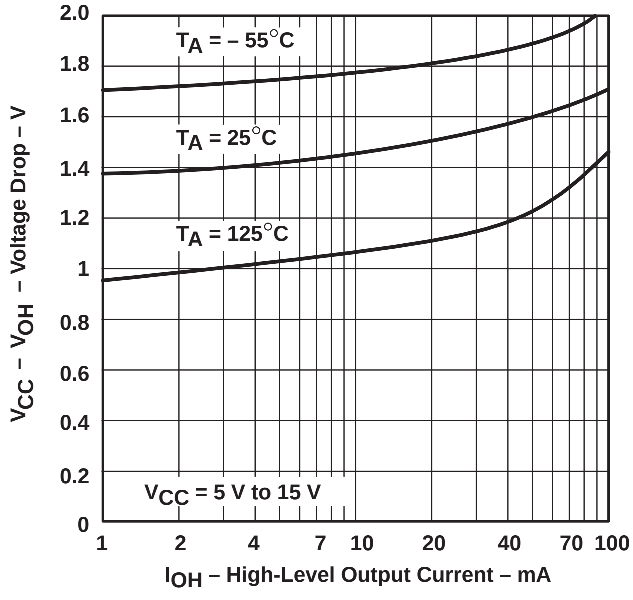


Figure 4

---

† Data for temperatures below 0°C and above 70°C are applicable for SE555-series circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT vs SUPPLY VOLTAGE

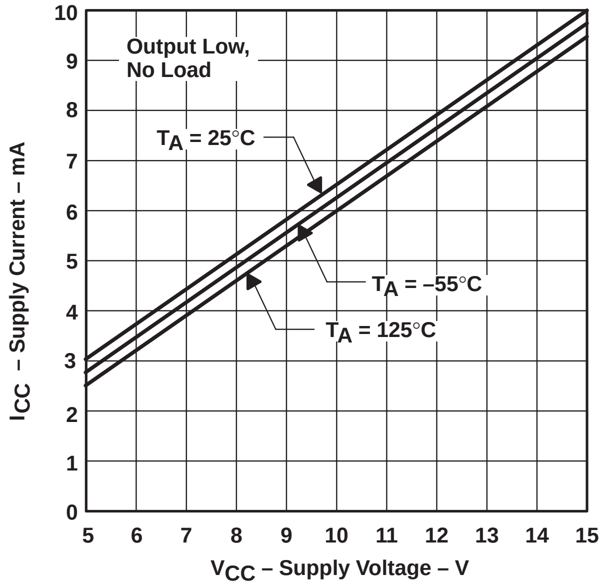


Figure 5

NORMALIZED OUTPUT PULSE DURATION (MONOSTABLE OPERATION) vs SUPPLY VOLTAGE

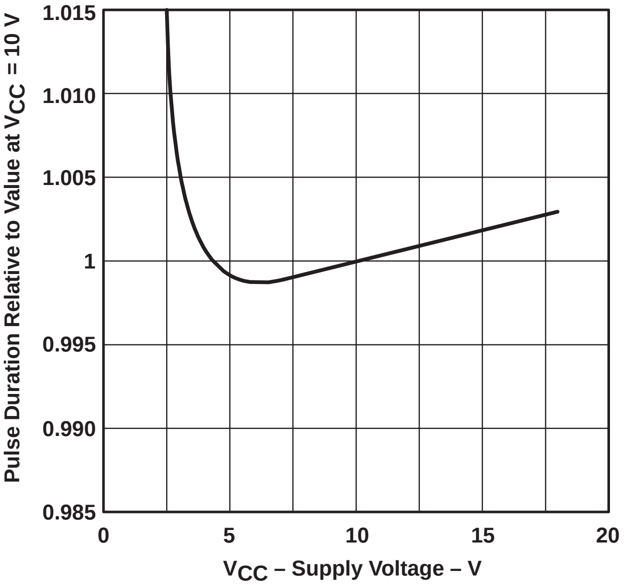


Figure 6

NORMALIZED OUTPUT PULSE DURATION (MONOSTABLE OPERATION) vs FREE-AIR TEMPERATURE

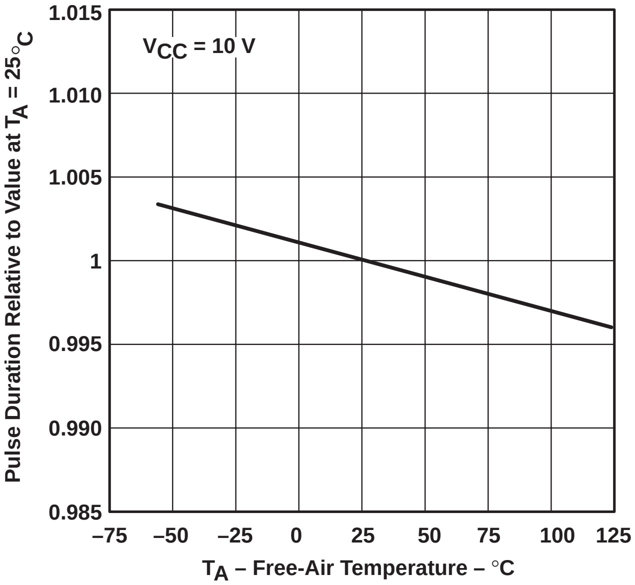


Figure 7

PROPAGATION DELAY TIME vs LOWEST VOLTAGE LEVEL OF TRIGGER PULSE

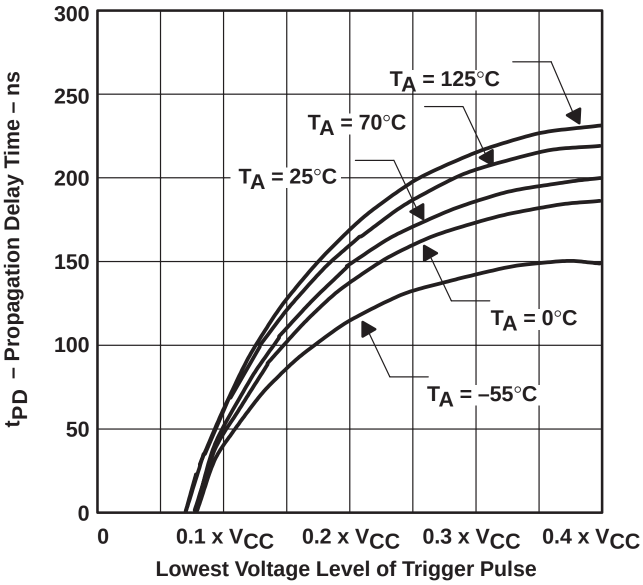


Figure 8

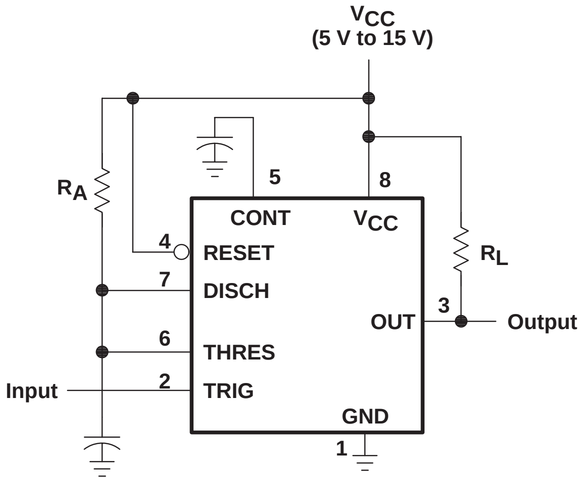
---

† Data for temperatures below 0°C and above 70°C are applicable for SE555-series circuits only.

APPLICATION INFORMATION

monostable operation

For monostable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to TRIG sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of THRES input. If TRIG has returned to a high level, the output of the threshold comparator will reset the flip-flop ($\overline{Q}$ goes high), drive the output low, and discharge C through Q1.



Pin numbers shown are for the D, JG, and P packages.

Figure 9. Circuit for Monostable Operation

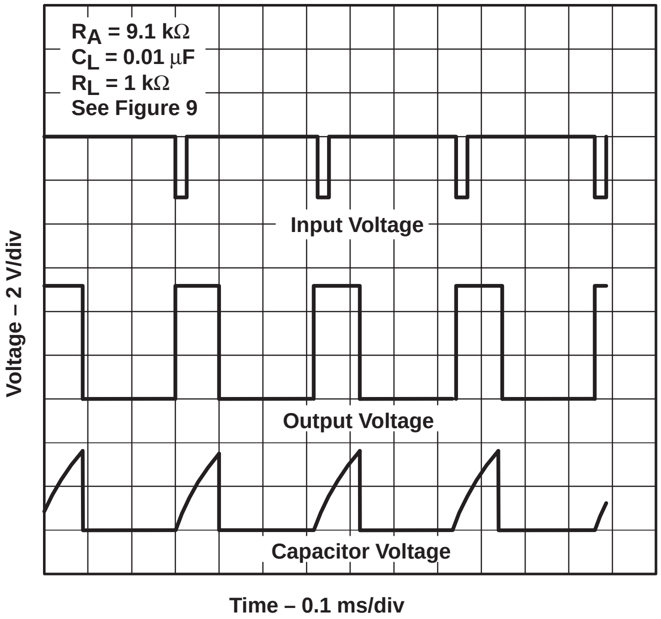


Figure 10. Typical Monostable Waveforms

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1 R_A C$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and re-initiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC}.

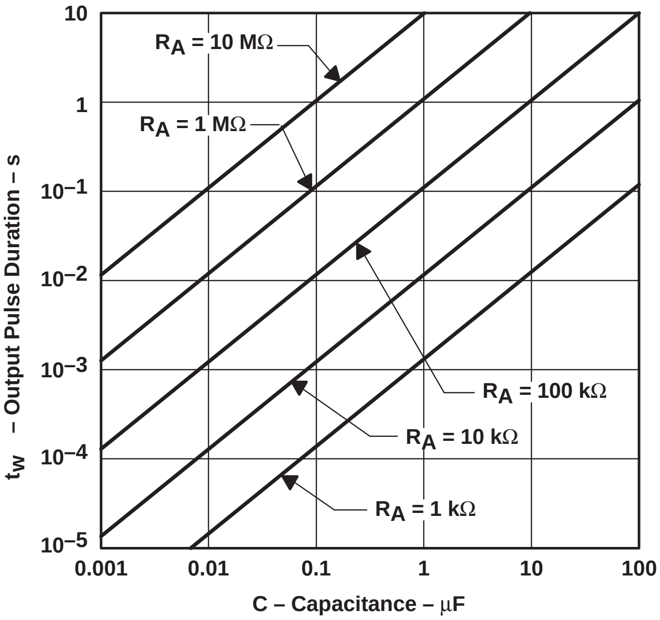


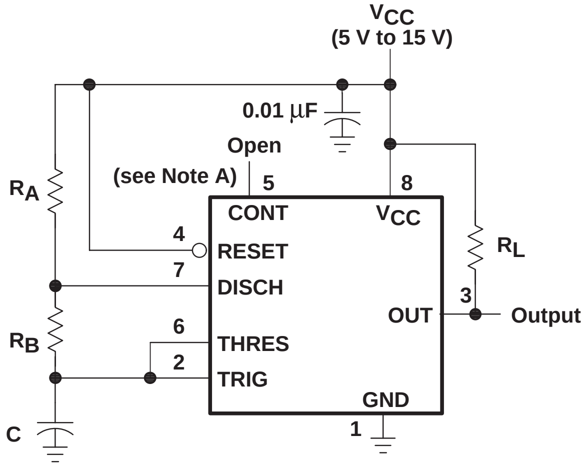
Figure 11. Output Pulse Duration vs Capacitance

APPLICATION INFORMATION

astable operation

As shown in Figure 12, adding a second resistor, $R_{B,}$ to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and $R_{B.}$

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \bullet V_{CC}$) and the trigger-voltage level ($\approx 0.33 \bullet V_{CC}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, and P packages.

NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

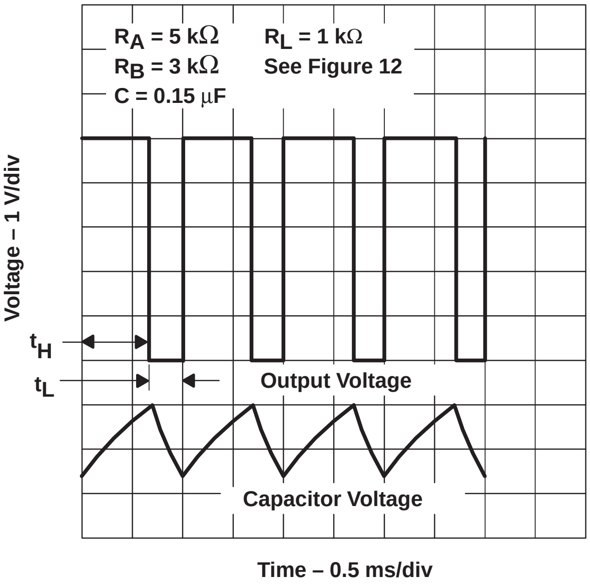


Figure 13. Typical Astable Waveforms

APPLICATION INFORMATION

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693\ (R_A + R_B)\ C$$
$$t_L = 0.693\ (R_B)\ C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693\ (R_A + 2R_B)\ C$$
$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)\ C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

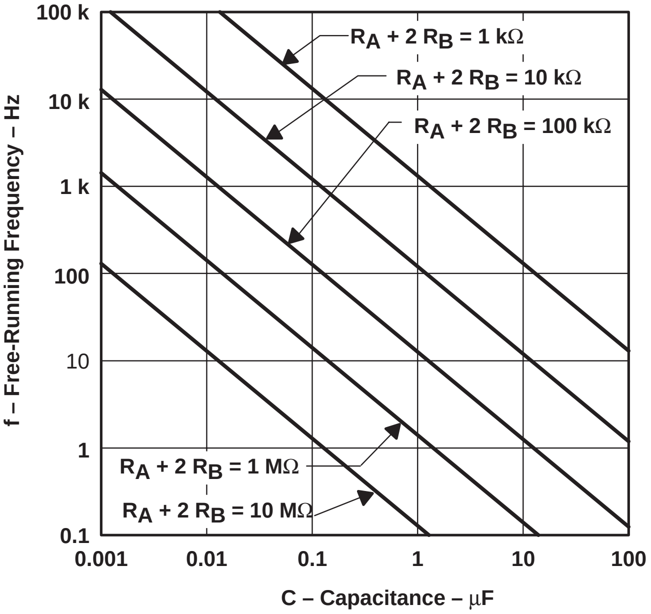
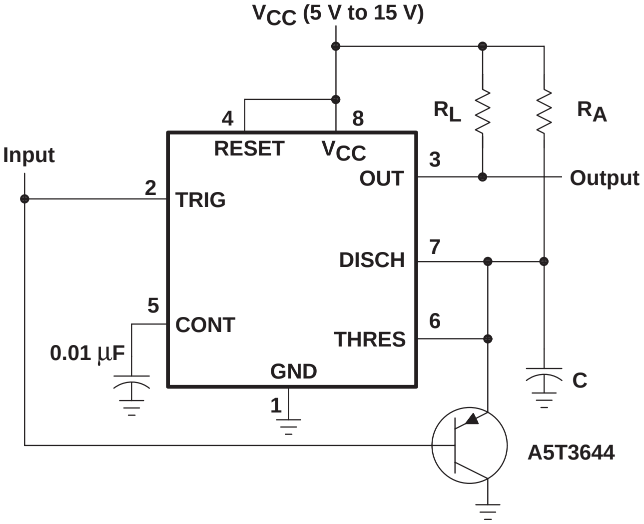


Figure 14. Free-Running Frequency

missing-pulse detector

The circuit shown in Figure 15 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 16.



Pin numbers shown are shown for the D, JG, and P packages.

Figure 15. Circuit for Missing-Pulse Detector

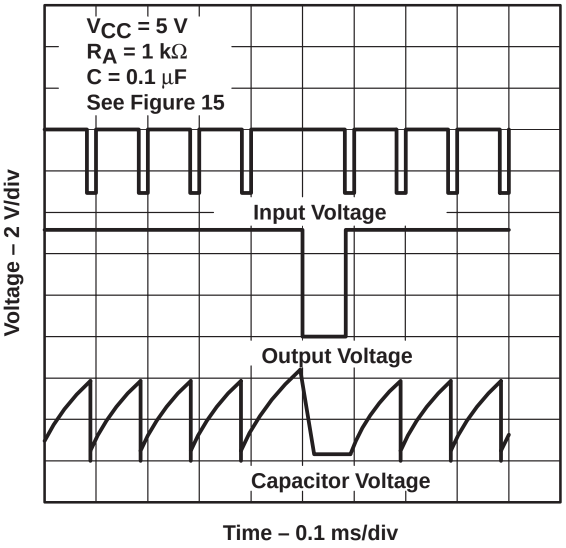


Figure 16. Circuit for Missing-Pulse Detector

APPLICATION INFORMATION

frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

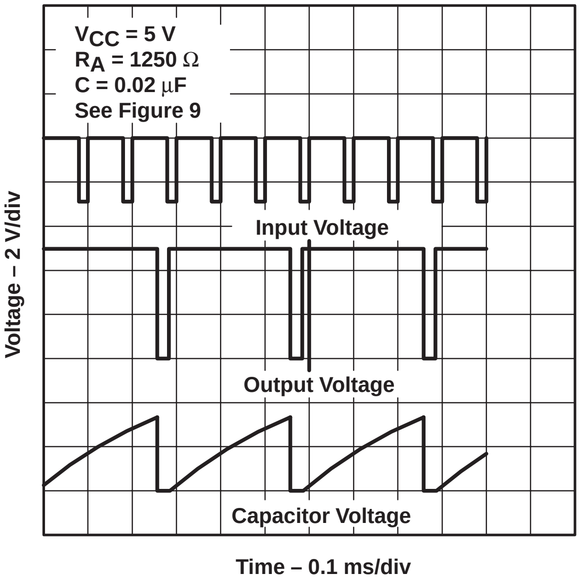
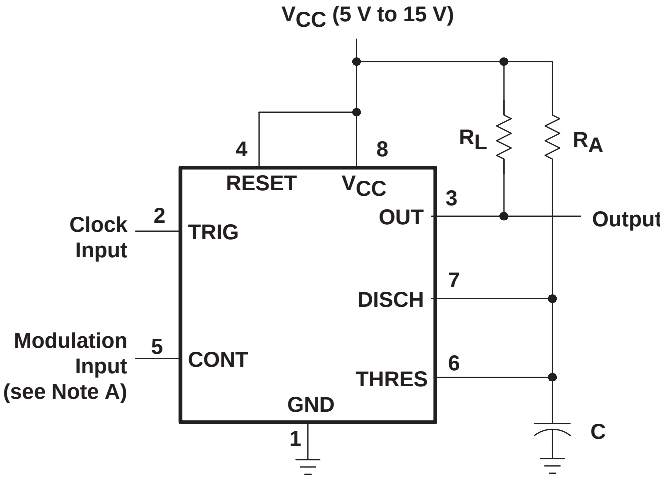


Figure 17. Divide-By-Three Circuit Waveforms

pulse-width modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is illustrated, any wave shape could be used.

APPLICATION INFORMATION



Pin numbers shown are for the D, JG, and P packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

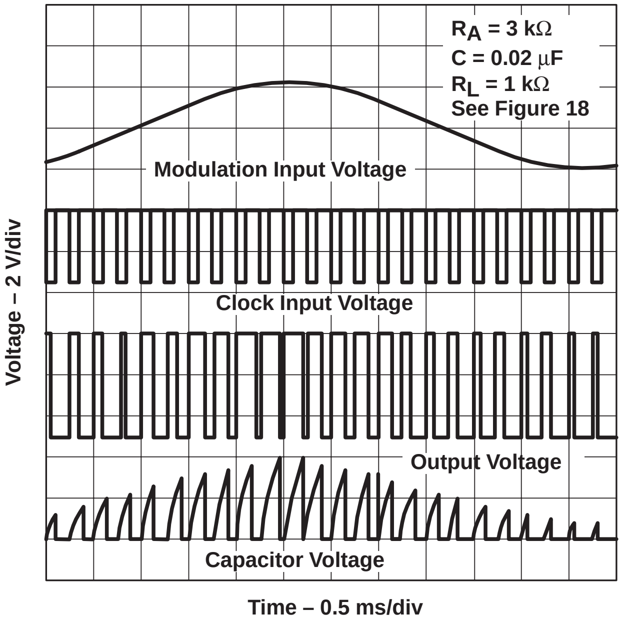
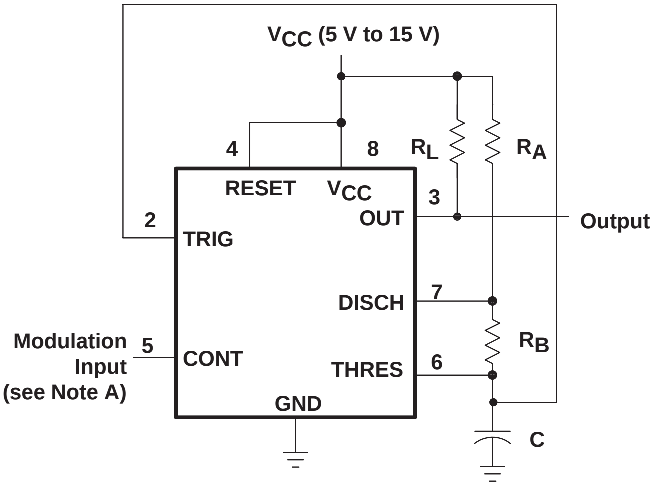


Figure 19. Pulse-Width Modulation Waveforms

pulse-position modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage, and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



Pin numbers shown are for the D, JG, and P packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

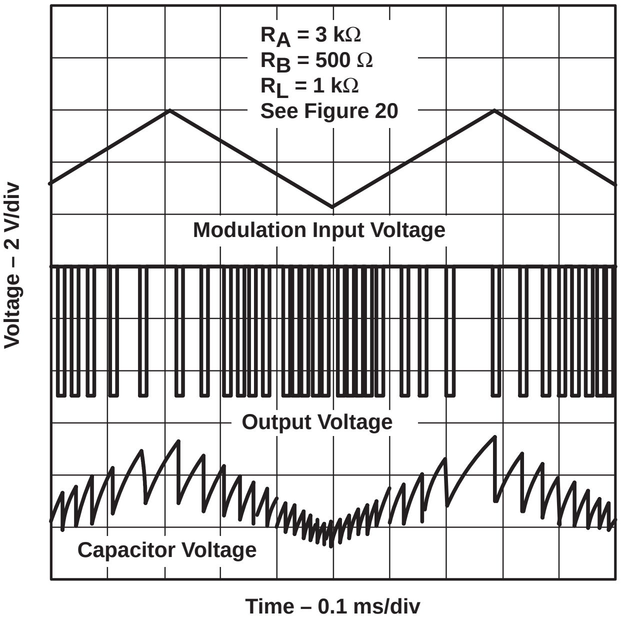
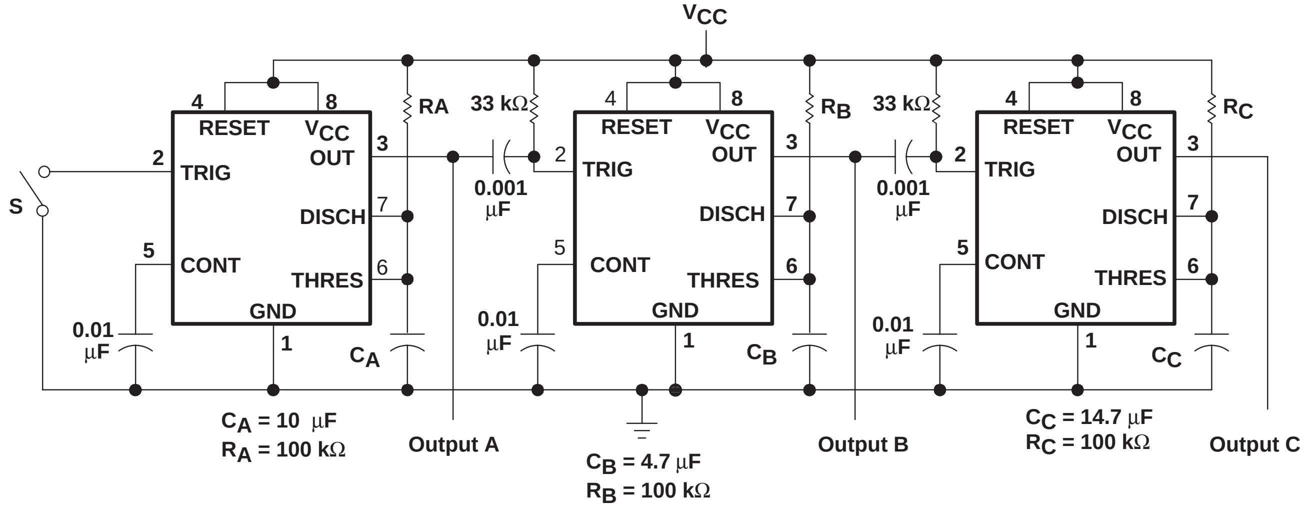


Figure 21. Pulse-Position-Modulation Waveforms

APPLICATION INFORMATION

sequential timer



S closes momentarily at t = 0.
Pin numbers shown are for the D, JG, and P packages.

Figure 22. Sequential Timer Circuit

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 shows a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.

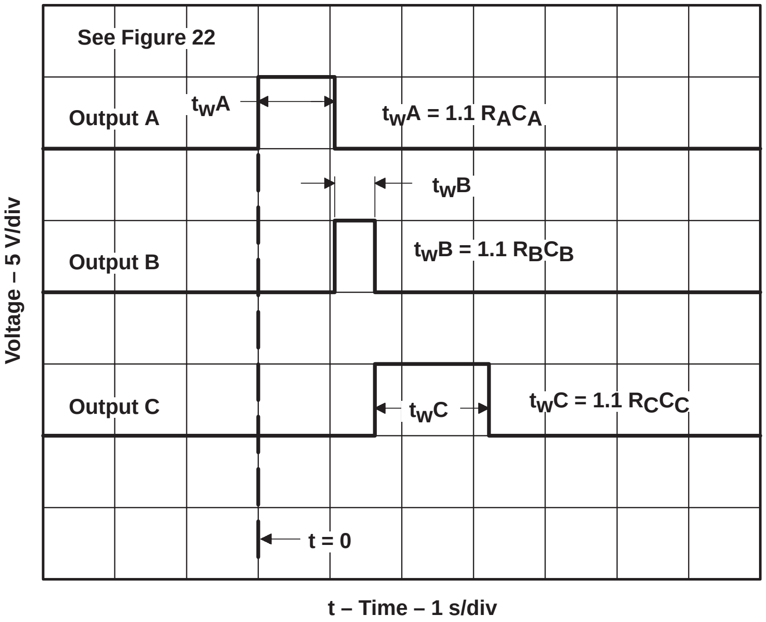


Figure 23. Sequential Timer Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated