WINSTAR Display

OLED SPECIFICATION

Model No:

WEO009664ALPP3N00000

Contents

SPECIFICATION Ver:A

CUSTOMER :

MODULE NO. : WEO009664ALPP3N00000

APPROVED BY: (FOR CUSTOMER USE ONLY)	**PCB VERSION:** **DATA:**

SALES BY	**APPROVED BY**	**CHECKED BY**	**PREPARED BY**
ISSUED DATE:			

MODLE NO：

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2012.07.03		First issue
A	2012.08.27	19	Correct Reliability

1. Basic Specifications

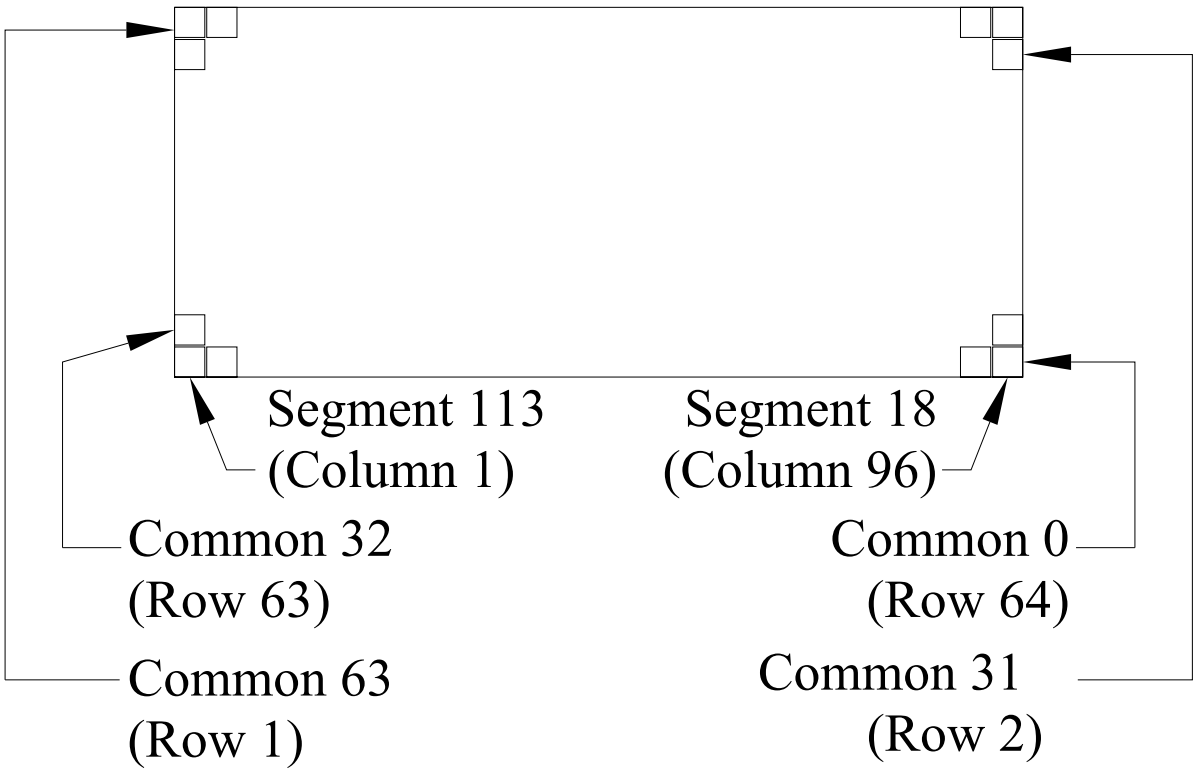
1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Display Color: Monochrome (Yellow)
3) Drive Duty: 1/64 Duty

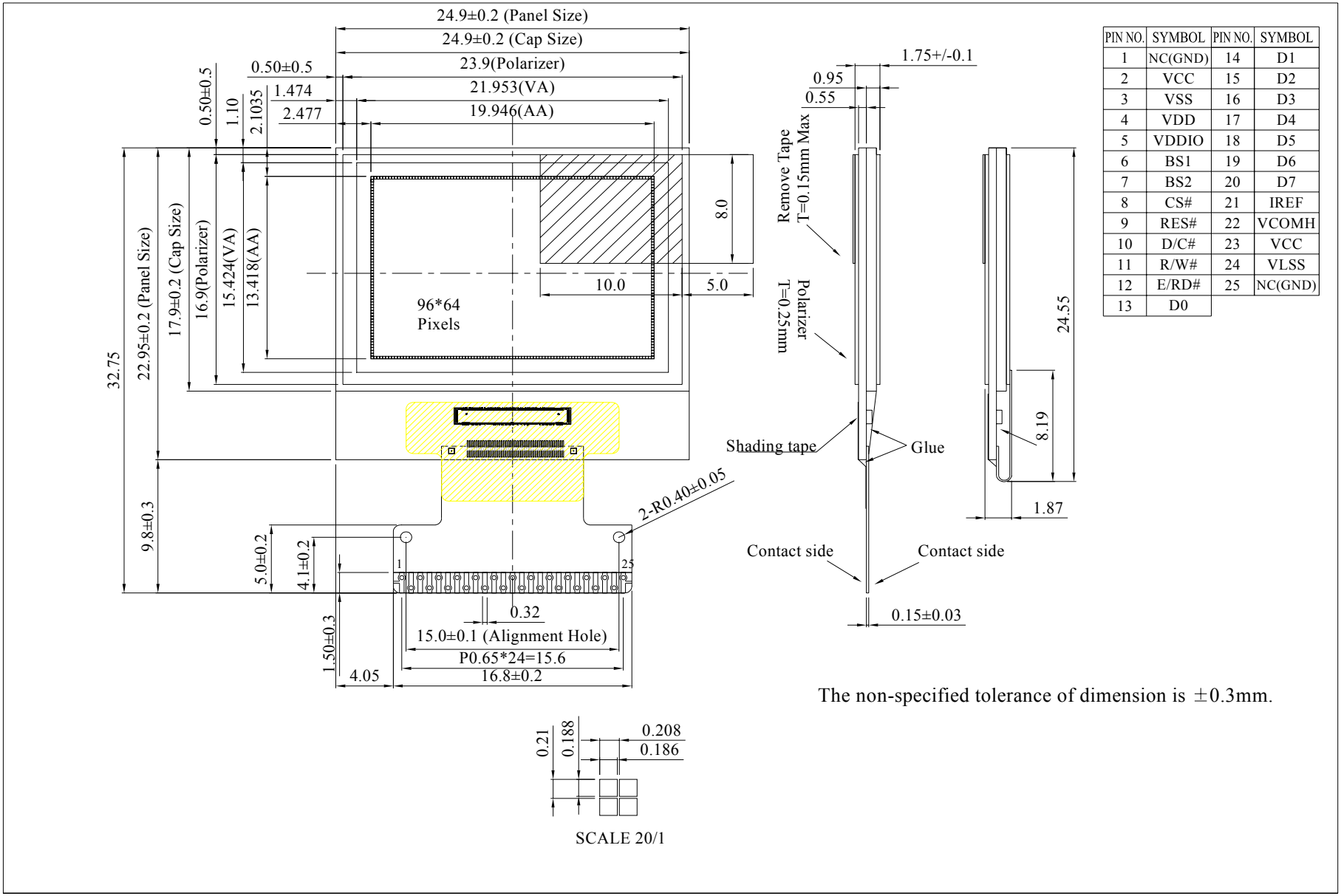
1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 96 × 64
3) Panel Size: 24.9 × 22.95 × 1.75 (mm)
4) Active Area: 19.946 × 15.424 (mm)
5) Pixel Pitch: 0.208 × 0.21 (mm)
6) Pixel Size: 0.186 × 0.188 (mm)

1.3 Active Area & Pixel Construction



1.4 Mechanical Drawing



PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	NC(GND)	14	D1
2	VCC	15	D2
3	VSS	16	D3
4	VDD	17	D4
5	VDDIO	18	D5
6	BS1	19	D6
7	BS2	20	D7
8	CS#	21	IREF
9	RES#	22	VCOMH
10	D/C#	23	VCC
11	R/W#	24	VLSS
12	E/RD#	25	NC(GND)
13	D0		

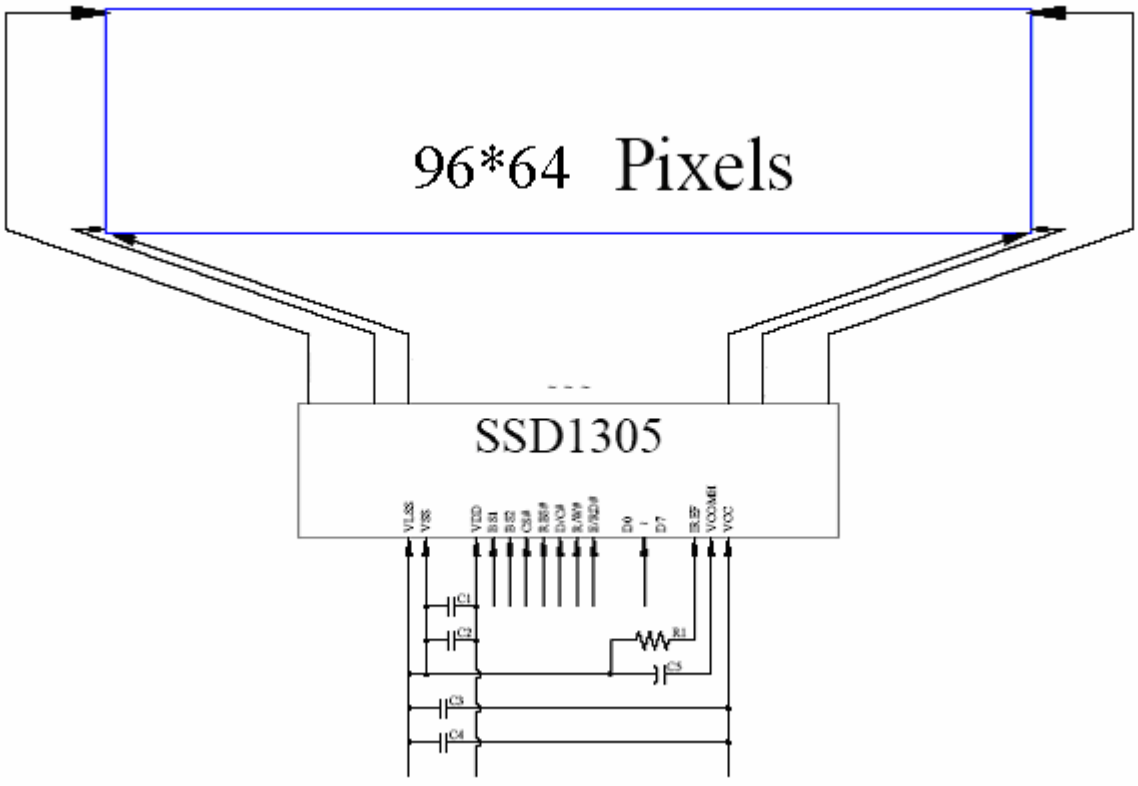
The non-specified tolerance of dimension is ±0.3mm.

1.5 Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1.</td><td>N.C.
(GND)</td><td>-</td><td>ReservedPin(SupportingPin)
The supporting pins can reduce the influences fromstresses on the function pins. These pins must beconnected to external ground.</td></tr>
<tr><td>2.</td><td>VCC</td><td>P</td><td>PowerSupplyforOLED Panel
This is the most positive voltage supply pin of the chip.It must be supplied externally.</td></tr>
<tr><td>3.</td><td>VSS</td><td>P</td><td>GroundofLogicCircuit
This is a ground pin. It also acts as a reference for thelogic pins. It must be connected to external ground.</td></tr>
<tr><td>4.</td><td>VDD</td><td>P</td><td>PowerSupplyforLogicCircuit
This is a voltage supply pin. It must be connected toexternal source.</td></tr>
<tr><td>5.</td><td>VDDIO</td><td>P</td><td>Power supply for interface logic level.
It should be match with MCU interface voltage level. VDDIO must always be equal or lower than VDD.</td></tr>
<tr><td>6.
7.</td><td>BS1
BS2</td><td>I</td><td>CommunicatingProtocolSelect
These pins are MCU interface selection input. See thefollowing table:
<table>
<tr><td></td><td>68XX-parallel</td><td>80XX-parallel</td><td>Serial</td><td>I2C</td></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>8.</td><td>CS#</td><td>I</td><td>ChipSelect
This pin is the chip select input. The chip is enabled forMCU communication only when CS# is pulled low.</td></tr>
<tr><td>9.</td><td>RES#</td><td>I</td><td>PowerResetforControllerandDriver
This pin is reset signal input. When the pin is low,initialization of the chip is executed.</td></tr>
<tr><td>10.</td><td>D/C#</td><td>I</td><td>Data/CommandControl
This pin is Data/Command control pin. When the pin ispulled high, the input at D7~D0 is treated as display data.When the pin is pulled low, the input at D7~D0 will betransferred to the command register. For detailrelationship to MCU interface signals, please refer to theTiming Characteristics Diagrams.
When the pin is pulled high and serial interface mode isselected, the data at SDIN is treated as data. When it ispulled low, the data at SDIN will be transferredto thecommand register. In I2C mode, this pin acts as SA0 forslave address selection.</td></tr>
<tr><td>11.</td><td>R/W#</td><td>I</td><td>Read/WriteSelectorWrite
This pin is MCU interface input. When interfacing to a68XX-series microprocessor, this pin will be used asRead/Write (R/W#) selection input. Pull this pin to“High” for read mode and pull it to “Low” for writemode.
When 80XXinterface mode is selected, this pin will bethe Write (WR#) input. Data write operation is initiatedwhen this pin is pulled low and the CS# is pulled low.</td></tr>
<tr><td>12.</td><td>E/RD#</td><td>I</td><td>Read/WriteEnableorRead
This pin is MCU interface input. When interfacing to a68XX-series microprocessor, this pin will be used as theEnable (E) signal. Read/write operation is initiated whenthis pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pinreceives the Read (RD#) signal. Data read operation isinitiated when this pin is pulled low</td></tr>
</table>

			and CS# is pulledlow.
13. **14.** **15.** **16.** **17.** **18.** **19.** **20.**	D0~D7	I/O	HostDataInput/OutputBus These pins are 8-bit bi-directional data bus to beconnected to the microprocessor's data bus. Whenserialmode is selected, D1 will be the serial data input SDINand D0 will be the serial clock input SCLK. When I2Cmode is selected, D2 & D1 should be tired together andserve as SDAout & SDAin in application and D0 is theserial clock input SCL.
21.	IREF	I	CurrentReferenceforBrightnessAdjustment This pin is segment current reference pin. A resistorshould be connected between this pin and VSS. Set thecurrent lower than 10μA.
22.	VCOMH	O	VoltageOutputHighLevelforCOMSignal This pin is the input pin for the voltage output high levelfor COM signals. A capacitor should be connectedbetween this pin and VSS.
23.	VCC	P	PowerSupplyforOLEDPanel This is the most positive voltage supply pin of the chip.It must be supplied externally.
24.	VLSS	P	GroundofAnalogCircuit This is an analog ground pin. It should be connected to VSSexternally.
25.	N.C. (GND)	-	ReservedPin(SupportingPin) The supporting pins can reduce the influences fromstresses on the function pins. These pins must beconnected to external ground.

1.6 Block Diagram



MCU Interface Selection: BS1 and BS2

Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C3: 0.1µF

C2: 4.7µF

C4: 10µF

C5: 4.7µF / 25V Tantalum Capacitor

R1: 910kΩ, R1 = (Voltage at IREF - VSS) / IREF

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	15	V	1, 2
Operating Temperature	T_{OP}	-40	+80	°C	-
Storage Temperature	T_{STG}	-40	+80	°C	-

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer (Note 3)	80	100	-	cd/m^2
C.I.E. (Yellow) Dark Room Contrast	(x) (y) CR	With Polarizer	0.44 0.46 -	0.48 0.50 >2000:1	0.52 0.54 -	degree
View Angle			>160	-	-	

Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12.5V.

Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		2.4	2.8	3.5	V
Supply Voltage for Display High Level Input	V_{CC} V_{IH}	Note 3 I_{OUT} = 100μA, 3.3MHz	12.0 0.8×V_{DD}	12.5 -	13.0 V_{DD}	V V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD} Operating Current for V_{CC}	I_{DD} I_{CC}	Note 4	- -	180 20	300 25	μA mA
		Note 5	-	28	35	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	5	μA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 4: V_{DD} = 2.8V, V_{CC} = 12.5V, 50% Display Area Turn on.

Note 5: V_{DD} = 2.8V, V_{CC} = 12.5V, 100% Display Area Turn on.

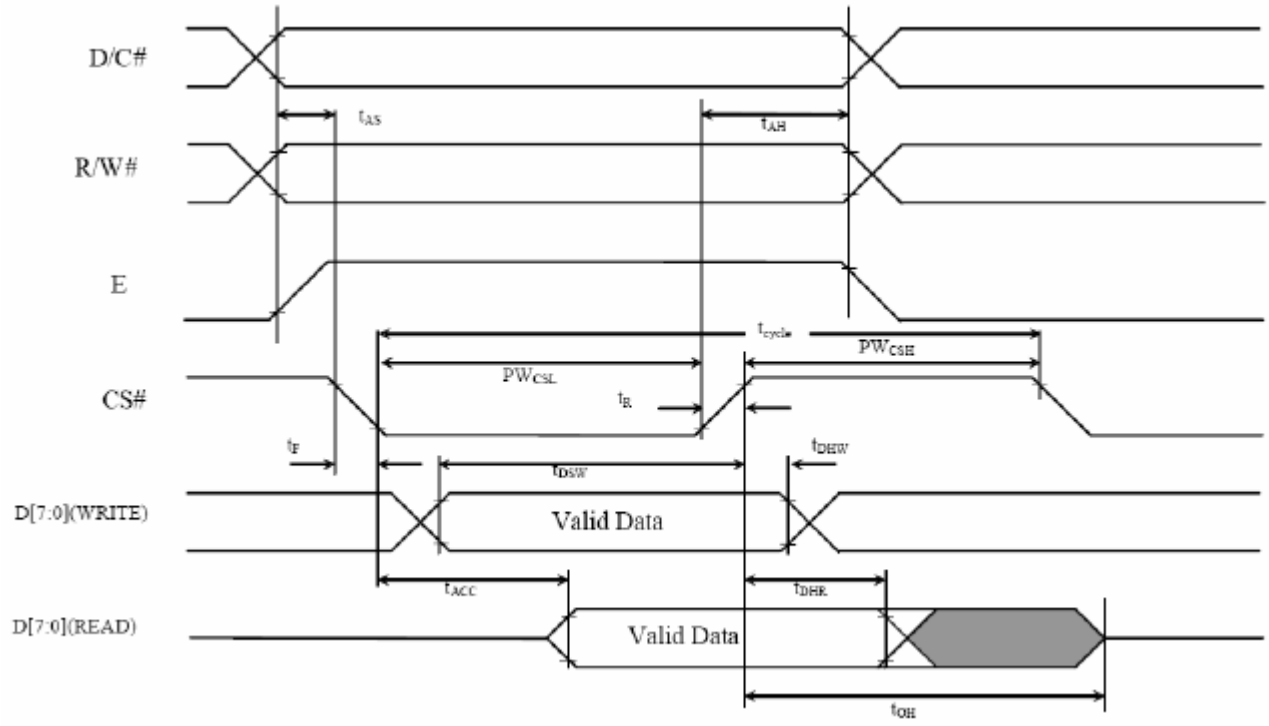
* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	System Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

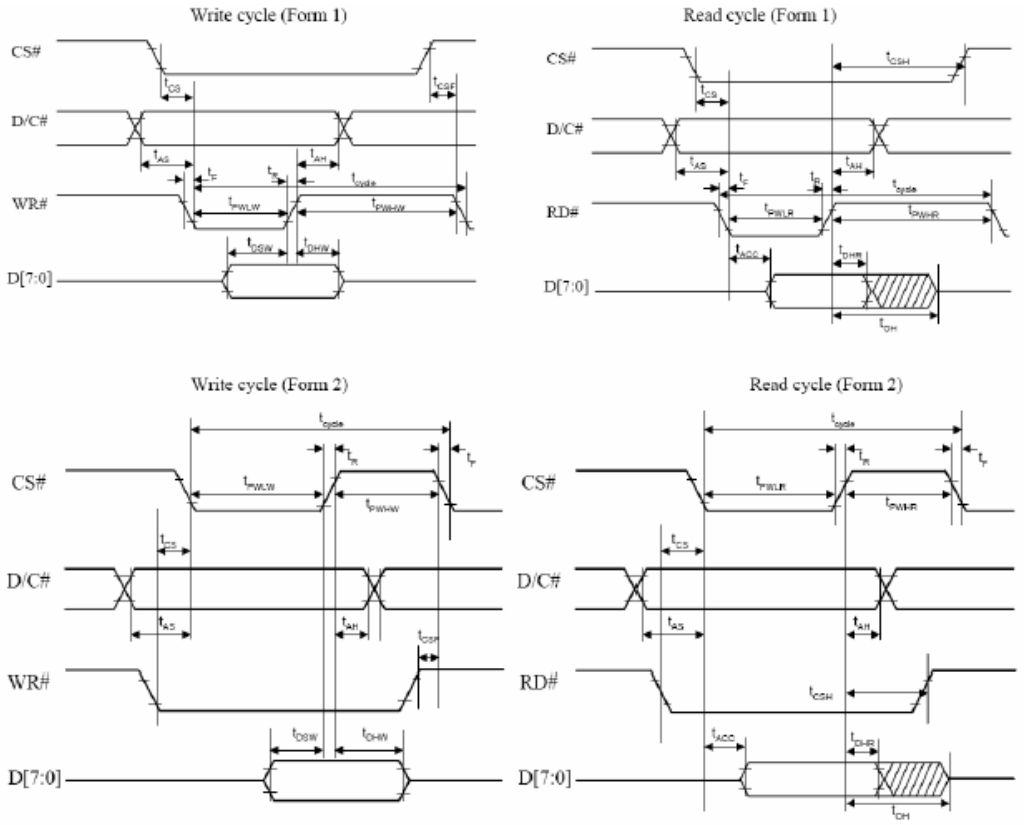
* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25°C)



3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS} t_{AH}	Address Setup Time Address Hold Time	10 0	- -	ns ns
t_{DSW} t_{DHW}	Write Data Setup Time Write Data Hold Time	40 7	- -	ns ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH} t_{CSF}	Chip Select Hold Time to Read Signal Chip Select Hold Time	0 20	- -	ns ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

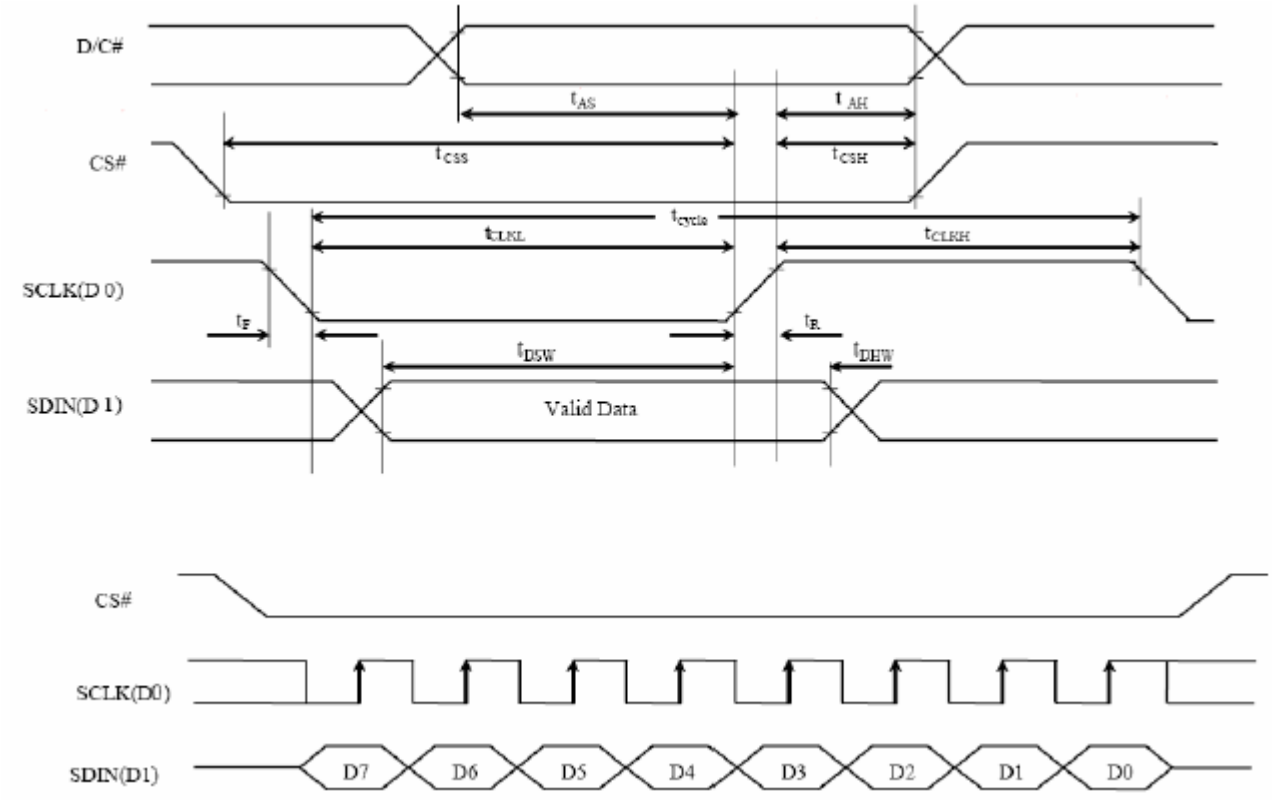
* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25°C)



3.3.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	50	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Serial Clock Low Time	100	-	ns
t_{CLKH}	Serial Clock High Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

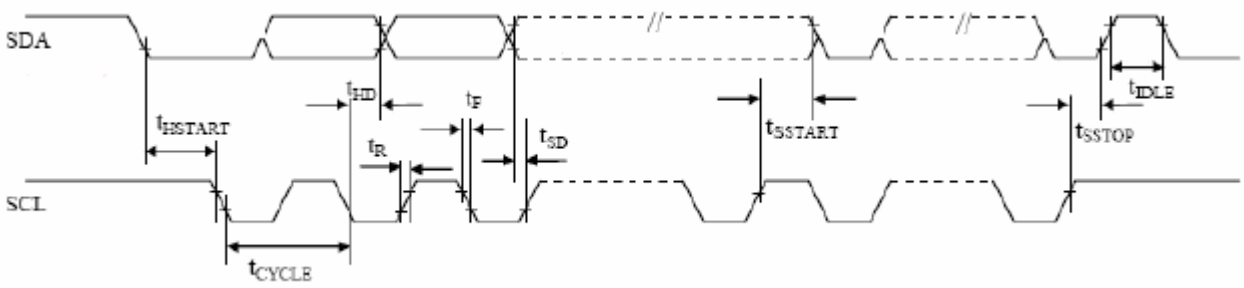
* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25°C)



3.3.4 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
	Data Hold Time (for "SDA_{OUT}" Pin)	0		
t_{HD}	Data Hold Time (for "SDA_{IN}" Pin)	300	-	ns
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	us

* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25°C)



4. Functional Specification

4.1. Commands

Refer to the Technical Manual for the SSD1305

4.2 Power down and Power up Sequence

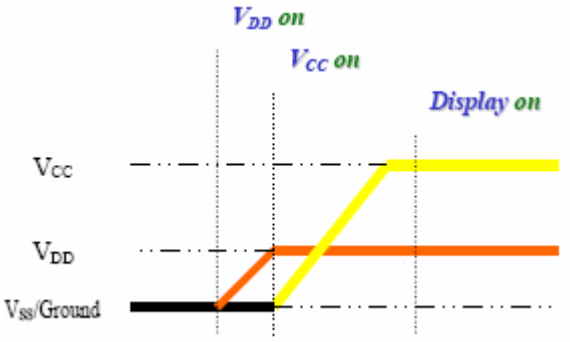
To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OLED panel enough time to complete the action of charge and discharge before/after the operation.

4.2.1 Power up Sequence:

1. Power up VDD
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VCC
6. Delay 100ms

(When VCC is stable)

7. Send Display on command

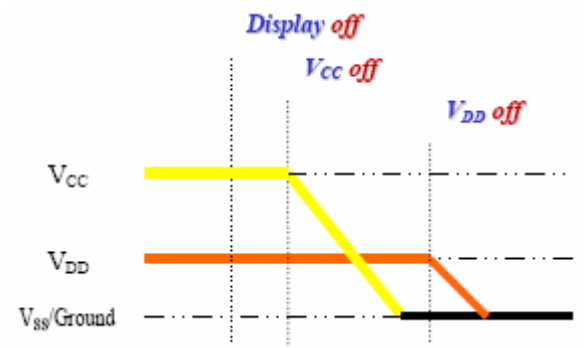


4.2.2 Power down Sequence:

1. Send Display off command
2. Power down VCC
3. Delay 100ms

(When VCC is reach 0 and panel
is completely discharges)

4. Power down VDD



4.3 Reset Circuit

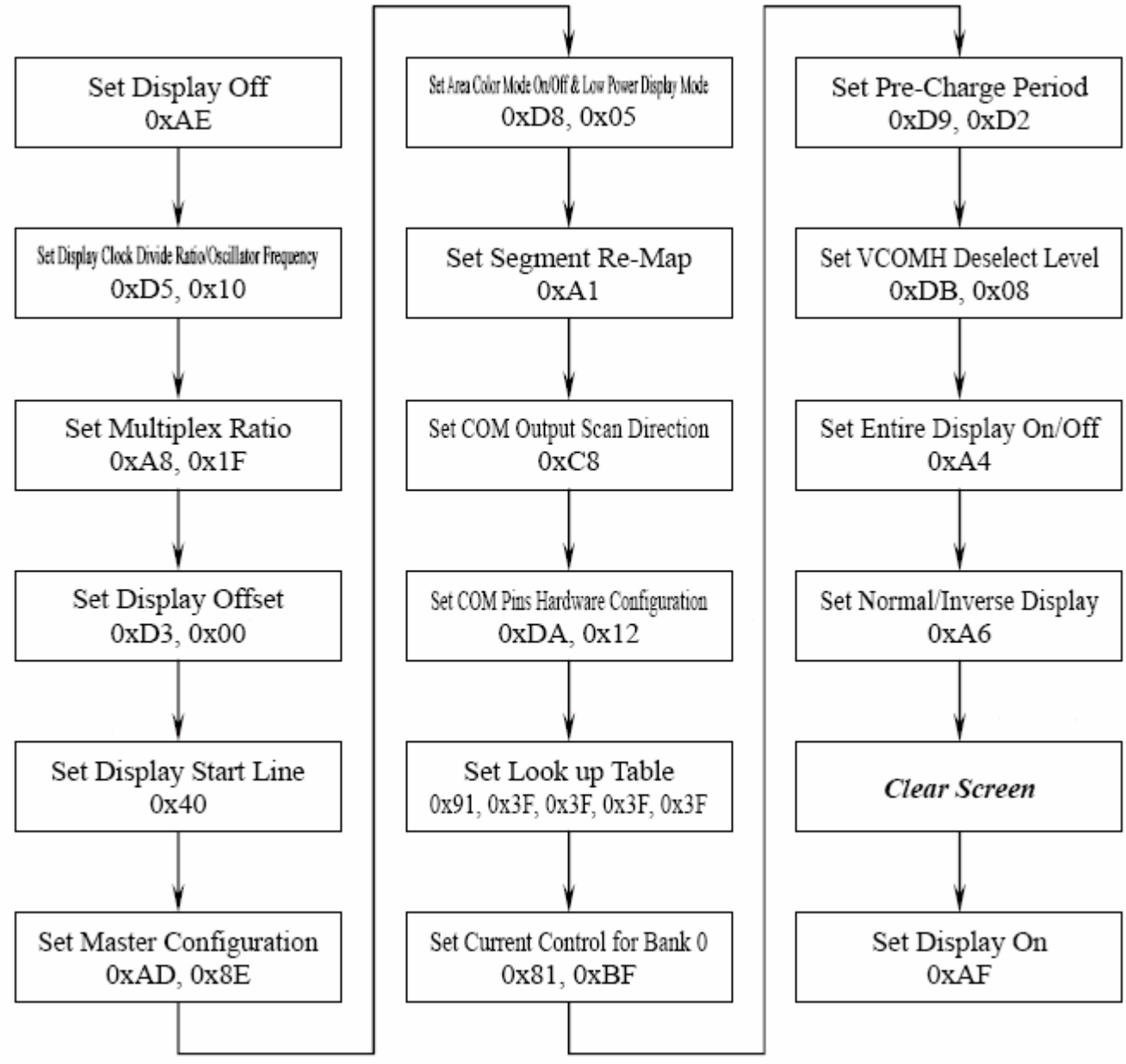
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 132×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80h
9. Normal display mode (Equivalent to A4h command)

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation Low Temperature Operation	80°C, 240 hrs -40°C, 240 hrs	The operational functions work.
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Storage	60°C, 90% RH, 240 hrs	
Thermal Shock	-40°C ~85°C, 100 cycles 30 mins dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness reached.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	50,000	-	hr	80.0 cd/m^2, 50% Checkerboard	6
Storage Life Time	50,000	-	hr	T_a = 25°C, 50% RH	-

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature: 23 ± 5°C

Humidity: 55 ± 15 %RH

Fluorescent Lamp: 30W

Distance between the Panel & Lamp: ≥ 50 cm

Distance between the Panel & Eyes of the Inspector: ≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

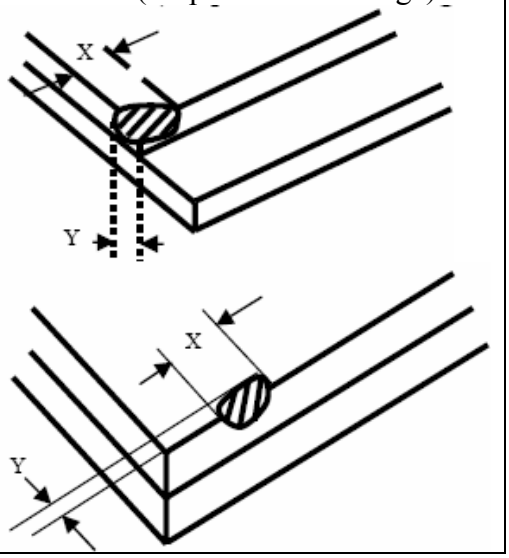
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

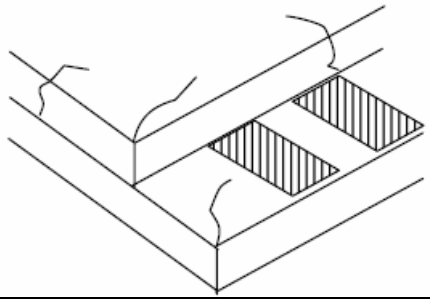
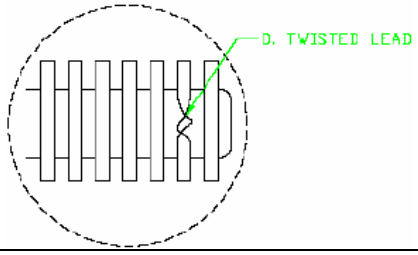
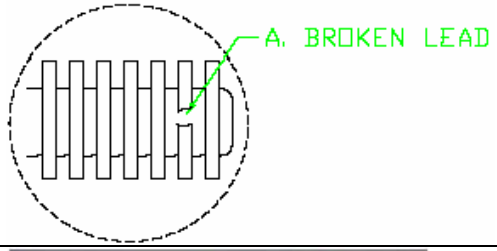
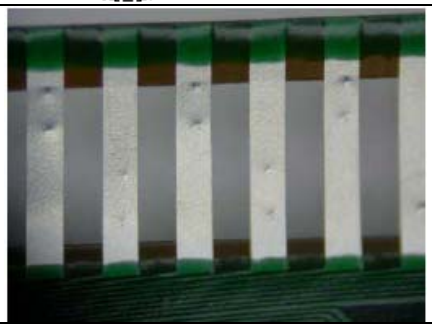
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

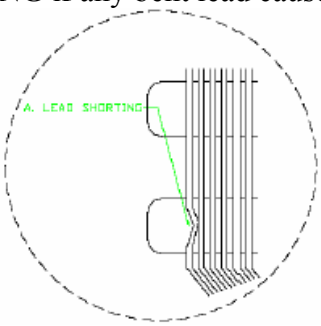
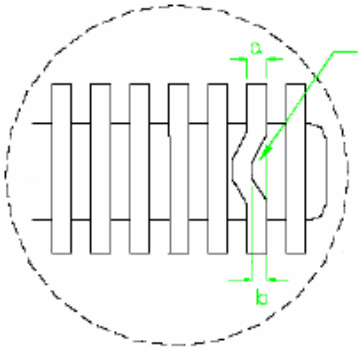
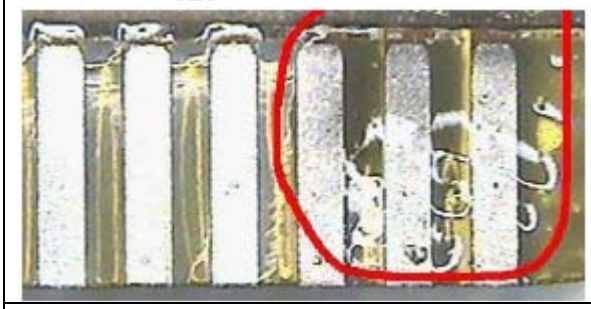
6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

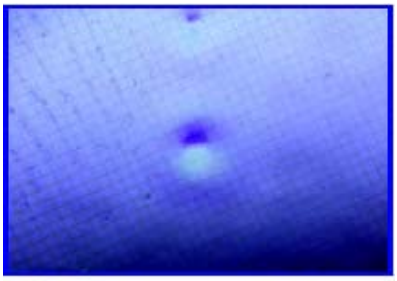
Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Prober Mark	Acceptable	

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check	**Item**	**ClassificationCriteria**
Terminal Lead Bent (Not Twist or Broken)	Minor	NG if any bent lead cause lead shorting. 
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol) Ink Marking on Back Side of panel (Exclude on Film)	Minor	NG for horizontally bent lead more than 50% of its width. 
	Minor	
	Acceptable	Ignore for Any

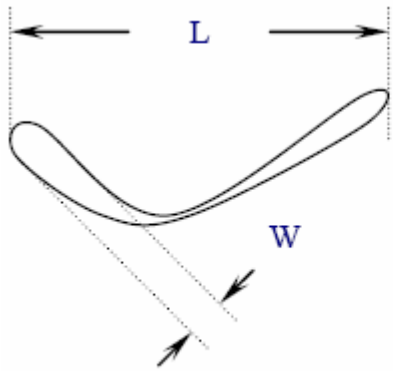
6.3.2 Cosmetic Check (Display Off) in Active Area

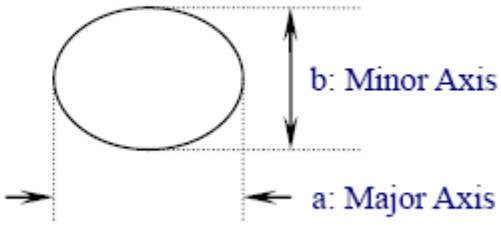
It is recommended to execute in clear room environment (class 10k) if actual in necessary

in necessary.	**Check Item**	**Classification**
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤0.1 Ignore W > 0.1, L ≤2 n ≤1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ≤0.1 Ignore 0.1 <Φ≤0.25 n ≤1 0.25 <Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ≤0.5 Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

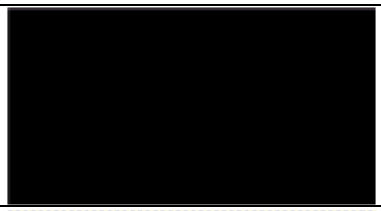
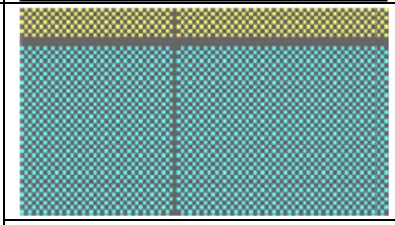
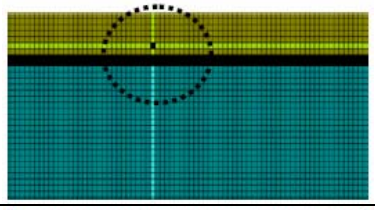
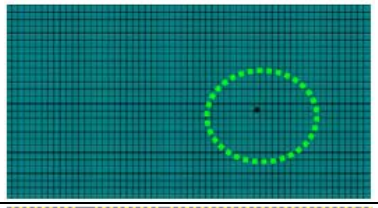
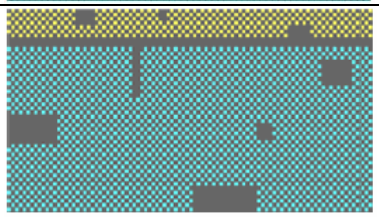
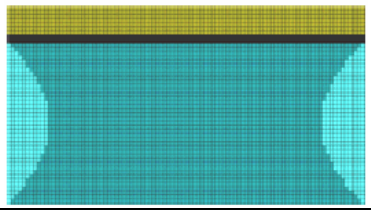
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2





6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display Missing Line	Major	
	Major Major	
Pixel Short		
Darker Pixel	Major	
Wrong Display Un-uniform	Major Major	 

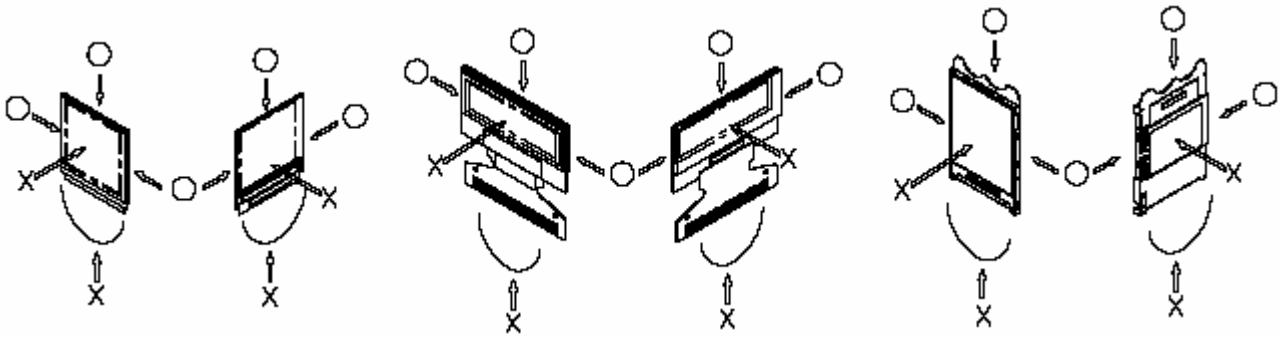
7. Precautions When Using These OLED Display Modules

7.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.
5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OLED display module very carefully when placing OLED display module into the system housing. Do not apply excessive stress or pressure to OLED display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OLED display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OLED display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OLED display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.

* To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
* Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

7.2 Storage Precautions

1) When storing OLED display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Winstar Display Co., Ltd.)
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

7.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.

2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.

3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)

4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.

5) As for EMI, take necessary measures on the equipment side basically.

6) When fastening the OLED display module, fasten the external plastic housing section.

7) If power supply to the OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.

8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1305 * Connection (contact) to any other potential than the above may lead to rupture of the IC.

7.4 Precautions when disposing of the OLED display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

7.5 Other Precautions

1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OLED display module, the OLED driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OLED driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.
4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.