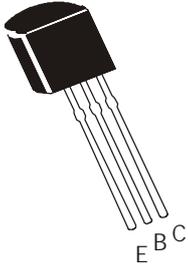


NPN SILICON PLANAR EPITAXIAL SWITCHING TRANSISTORS

2N4400 / 2N4401



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General Purpose Switching And Amplifier Applications

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

DESCRIPTION	SYMBOL	VALUE	UNITS
Collector Emitter Voltage	V_{CEO}	40	V
Collector Base Voltage	V_{CBO}	60	V
Emitter Base Voltage	V_{EBO}	6.0	V
Collector Current Continuous	I_C	600	mA
Power Dissipation at $T_a=25^\circ\text{C}$	P_D	625	mW
Derate Above 25°C		5.0	mW/ $^\circ\text{C}$
Power Dissipation at $T_c=25^\circ\text{C}$	P_D	1.5	W
Derate Above 25°C		12	mW/ $^\circ\text{C}$
Operating And Storage Junction Temperature Range	T_j, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL RESISTANCE

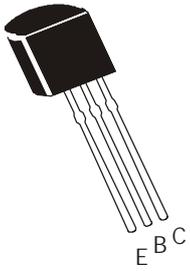
Junction to Case	$R_{th(j-c)}$	83.3	$^\circ\text{C/W}$
Junction to Ambient in free air	$R_{th(j-a)}$	200	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$ unless specified otherwise)

DESCRIPTION	SYMBOL	TEST CONDITION	MIN	MAX	UNITS
Collector Emitter Voltage	V_{CEO}	$I_C=1\text{mA}, I_B=0$	40		V
Collector Base Voltage	V_{CBO}	$I_C=100\mu\text{A}, I_E=0$	60		V
Emitter Base Voltage	V_{EBO}	$I_E=100\mu\text{A}, I_C=0$	6.0		V
Base Cut Off Current	I_{BEV}	$V_{CE}=35\text{V}, V_{EB}=0.4\text{V}$		100	nA
Collector Cut Off Current	I_{CEX}	$V_{CE}=35\text{V}, V_{EB}=0.4\text{V}$		100	nA
DC Current Gain	* h_{FE}	$I_C=0.1\text{mA}, V_{CE}=1\text{V}$	2N4400: -	2N4401: >20	
		$I_C=1\text{mA}, V_{CE}=1\text{V}$	>20	>40	
		$I_C=10\text{mA}, V_{CE}=1\text{V}$	>40	>80	
		$I_C=150\text{mA}, V_{CE}=1\text{V}$	50 - 150	100 - 300	
		$I_C=500\text{mA}, V_{CE}=2\text{V}$	>20	>40	

*Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

2N4400_4401Rev_1 071105E



TO-92
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ELECTRICAL CHARACTERISTICS (T_a=25°C unless specified otherwise)

DESCRIPTION	SYMBOL	TEST CONDITION	MIN	MAX	UNITS
Collector Emitter Saturation Voltage	*V _{CE (sat)}	I _C =150mA, I _B =15mA		0.40	V
		I _C =500mA, I _B =50mA		0.75	V
Base Emitter Saturation Voltage	*V _{BE (sat)}	I _C =150mA, I _B =15mA	0.75	0.95	V
		I _C =500mA, I _B =50mA		1.20	V

SMALL SIGNAL CHARACTERISTICS

DESCRIPTION	SYMBOL	TEST CONDITION	2N4400	2N4401	UNITS
Transistors Frequency	f _T	I _C =20mA, V _{CE} =10V, f=100MHz	>200	>250	MHz
Collector Base Capacitance	C _{cb}	V _{CB} =5V, I _E =0, f=100KHz	< 6.5		pF
Emitter Base Capacitance	C _{eb}	V _{EB} =0.5V, I _C =0, f=100KHz	<30		pF
Input Impedence	h _{ie}	I _C =1mA, V _{CE} =10V, f=1KHz	0.5 - 7.5	1.0 -15	kΩ
Voltage Feedback Ratio	h _{re}	I _C =1mA, V _{CE} =10V, f=1KHz	0.1 - 8.0		x10 ⁻⁴
Small Signal Current Gain	h _{fe}	I _C =1mA, V _{CE} =10V, f=1KHz	20 - 250	40 - 500	
Out put Adimttance	h _{oe}	I _C =1mA, V _{CE} =10V, f=1KHz	1.0 - 30		μmhos

SWITCHING Time

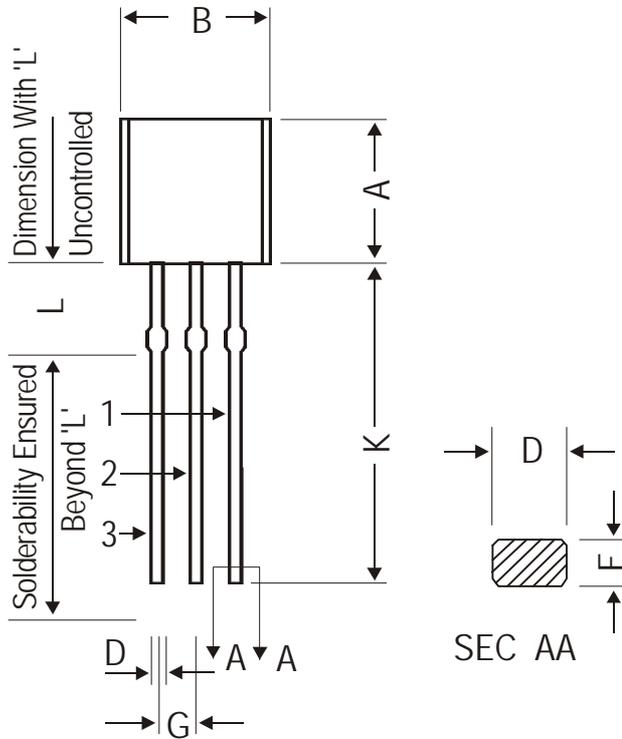
Delay time	t _d	V _{CC} =30, V _{EB} =2V	< 15	ns
Rise time	t _r	I _C =150mA, I _{B1} =15mA	< 20	ns
Storage time	t _s	V _{CC} =30V, I _C =150mA	< 225	ns
Fall time	t _f	I _{B1} =15mA, I _{B2} =15mA	< 30	ns

*Pulse Test: Pulse Width ≤ 300ms, Duty Cycle ≤ 2%

2N4400_4401Rev_1 071105E

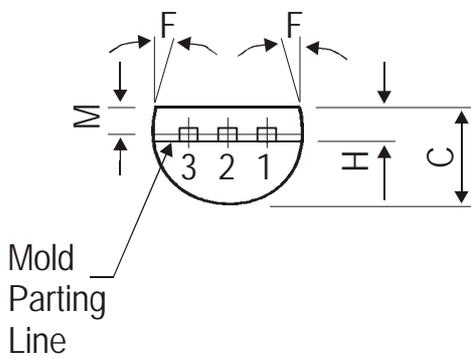
TO-92
Plastic Package
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TO-92 Plastic Package



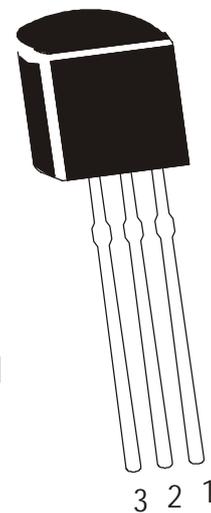
DIM	MIN.	MAX.
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.41	0.55
E	0.35	0.50
F	5 DEG	
G	1.14	1.40
H	1.20	1.40
K	12.70	—
L	1.982	2.082
M	1.03	1.20

All dimensions are in mm



PIN CONFIGURATION

1. COLLECTOR
2. BASE
3. EMITTER



The TO-92 Package, Tape and Ammo Pack Drawings are correct as on the date of issue/revision of this Data Sheet.

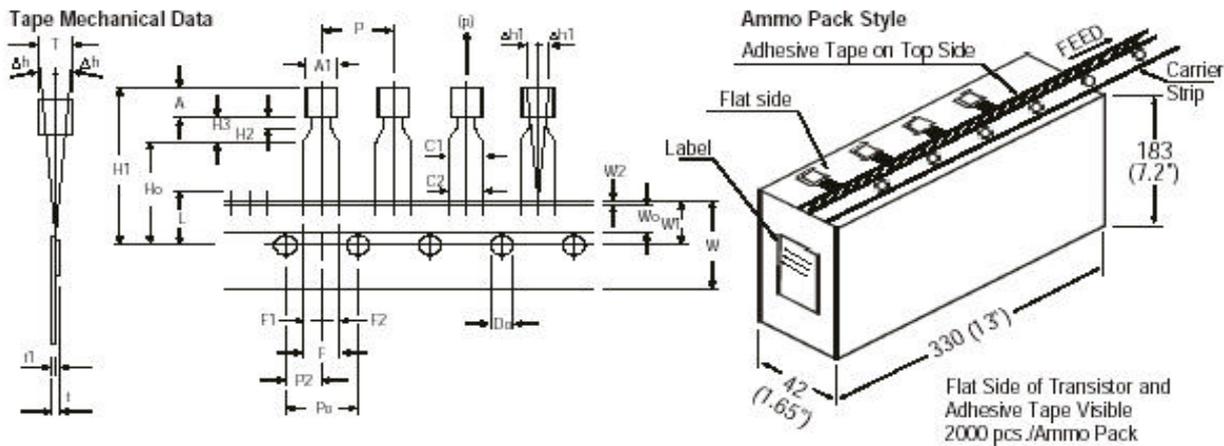
The currently valid dimensions and information, may please be confirmed from the TO-92 Drawing in the Packages and Packing Section of the Product Catalogue.

Packing Details

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Gr Wt
TO-92 Bulk	1K/polybag	200 gm/1K pcs	3" x 7.5" x 7.5"	5K	17" x 15" x 13.5"	80K	23 kgs
TO-92 T&A	2K/ammo box	645 gm/2K pcs	12.5" x 8" x 1.8"	2K	17" x 15" x 13.5"	32K	12.5 kgs

TO-92
Plastic Package
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TO-92 Tape and Ammo Pack



All dimensions are in mm

ITEM	SYMBOL	SPECIFICATION			
		MIN.	NOM.	MAX.	TOL.
BODY WIDTH	A1	4.45		5.20	
BODY HEIGHT	A	4.32		5.33	
BODY THICKNESS	T	3.18		4.19	
PITCH OF COMPONENT	P		12.7		± 1.0
*1 FEED HOLE PITCH	Po		12.7		± 0.3
*2 FEED HOLE CENTRE TO COMPONENT CENTRE	P2		6.35		± 0.4
DISTANCE BETWEEN OUTER LEADS	F		5.08		+0.6 -0.2
*3 COMPONENT ALIGNMENT SIDE VIEW	Δh		0	1.0	
*4 COMPONENT ALIGNMENT FRONT VIEW	Δh1		0	1.3	
TAPE WIDTH	W		18		± 0.5
HOLD-DOWN TAPE WIDTH	W0		6		± 0.2
HOLE POSITION	W1		9		+0.7 -0.5
HOLD-DOWN TAPE POSITION	W2	0.0		0.7	
LEAD WIRE CLINCH HEIGHT	Ho		16		± 0.5
COMPONENT HEIGHT	H1			24.0	
LENGTH OF SNIPPED LEADS	L			11.0	
FEED HOLE DIAMETER	Do		4		± 0.2
*5 TOTAL TAPE THICKNESS	t			1.2	
LEAD - TO - LEAD DISTANCE	F1, F2	2.40		2.70	- 0.1
STAND OFF	H2	0.45		1.45	
CLINCH HEIGHT	H3			3.0	
LEAD PARALLELISM	C1 - C2			0.22	
PULL - OUT FORCE	(p)	6N			

NOTES

1. Maximum alignment deviation between leads will not to be greater than 0.2mm.
2. Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
3. Holddown tape will not exceed beyond the edge(s) of carrier tape and there shall be no exposure of adhesive.
4. There will be no more than three (3) consecutive missing components in a tape.
5. A tape trailer, having at least three feed holes are provided after the last component in a tape.
6. Splices should not interfere with the sprocket feed holes.

REMARKS

- *1 Cumulative pitch error 1.0 mm/20 pitch
- *2 To be measured at bottom of clinch
- *3 At top of body
- *4 At top of body
- *5 t1 0.3 – 0.6 mm

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

TO-92

Plastic Package

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Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Discrete Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Discrete Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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