Micro Support Devices

Order code	Manufacturer code	Description
82-0544	n/a	MAX1232CPA LOW POWER CMOS MICRO MONITOR

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19-3899, Rev 1, 2/91

MAXIM

MAX1232 Microprocessor Monitor

MAX1232

General Description

The MAX1232 microprocessor (µP) supervisory circuit provides µP "housekeeping" and power-supply supervision functions while consuming only 1/10th the power of the DS1232. The MAX1232 enhances circuit reliability in µP systems by monitoring the power supply, monitoring software execution, and providing a debounced manual reset input. The MAX1232 is a plug-in upgrade of the Dallas DS1232.

A reset pulse of at least 250ms duration is supplied on power-up, power-down, and low-voltage brown-out conditions (5% or 10% supply tolerances can be selected digitally). Also featured is a debounced manual reset input that forces the reset outputs to their active states for a minimum of 250ms. A digitally-programmable watchdog timer monitors software execution and can be programmed for timeout settings of 150ms, 600ms, or 1.2sec. The MAX1232 requires no external components.

Applications

Computers

Controllers

Intelligent Instruments

Automotive Systems

Critical µP Power Monitoring

Features

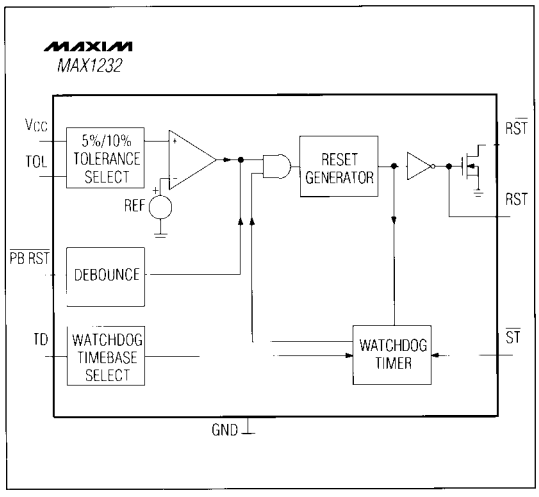
- ♦ **Consumes 1/10th the Power of the DS1232**
- ♦ **Precision Voltage Monitor - Adjustable +4.5V or +4.75V**
- ♦ **Power OK/Reset Pulse Width - 250ms Min**
- ♦ **No External Components**
- ♦ **Adjustable Watchdog Timer - 150ms, 600ms, or 1.2sec**
- ♦ **Debounced Manual Reset Input for External Overide**
- ♦ **Available in 8-pin DIP/Small Outline and 16-pin Wide Small Outline Packages**

Ordering Information

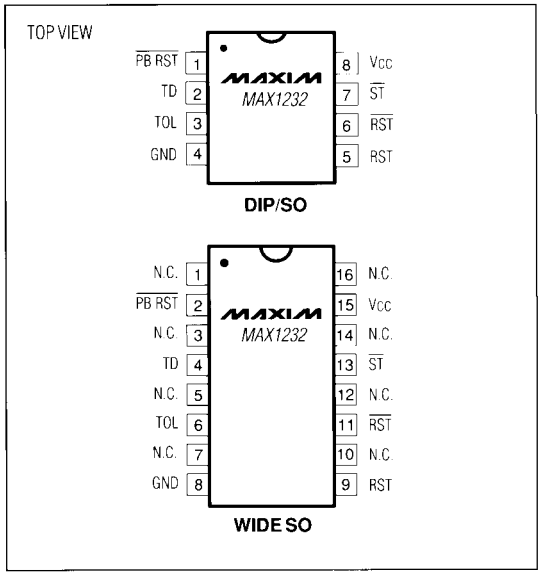
PART	TEMP. RANGE	PIN-PACKAGE
MAX1232CPA	0°C to +70°C	8 Plastic DIP
MAX1232CSA	0°C to +70°C	8 SO
MAX1232CWE	0°C to +70°C	16 Wide SO
MAX1232C/D	0°C to +70°C	Dice*
MAX1232EPA	-40°C to +85°C	8 Plastic DIP
MAX1232ESA	-40°C to +85°C	8 SO
MAX1232EWE	-40°C to +85°C	16 Wide SO
MAX1232MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Block Diagram



Pin Configuration



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin (with respect to GND) ..... -1V to +7V
Operating Temperature Ranges:
MAX1232C_ _ ..... 0°C to +70°C
MAX1232E_ _ ..... -40°C to +85°C
MAX1232M_ _ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(T_A = T_{MIN} to T_{MAX})

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
$\overline{ST}$ and $\overline{PB\ RST}$ Input High Level (Note 1)	V_{IH}		2.0		V_{CC} +0.3	V
$\overline{ST}$ and $\overline{PB\ RST}$ Input Low Level	V_{IL}		-0.3		+0.8	V

D.C. ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}; V_{CC} = +4.5V to +5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage $\overline{ST}$, TOL	I_{IL}		-1.0		+1.0	µA
Output Current RST	I_{OH}	V_{OH} = 2.4V	-1.0	-12		mA
Output Current RST, $\overline{RST}$	I_{OL}	V_{OL} = 0.4V	2.0	10		mA
Operating Current (Note 2)	I_{CC}			50	200	µA
V_{CC} 5% Trip Point (Note 3)	V_{CCTP}	TOL = GND	4.50	4.62	4.74	V
V_{CC} 10% Trip Point (Note 3)	V_{CCTP}	TOL = V_{CC}	4.25	4.37	4.49	V

CAPACITANCE (Note 4)

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance ST, TOL	C_{IN}				5	pF
Output Capacitance RST, $\overline{RST}$	C_{OUT}				7	pF

A.C. ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}; V_{CC} = +5V to ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PB $\overline{RST}$ (Note 5)	t_{PB}	Figure 3	20			ms
PB $\overline{RST}$ Delay	t_{PBD}	Figure 3	1	4	20	ms
Reset Active Time	t_{RST}		250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	Figure 4	75			ns
$\overline{ST}$ Timeout Period	t_{TD}	Figure 4 TD pin = 0V	62.5	150	250	ms
		TD pin = open	250	600	1000	
		TD pin = V_{CC}	500	1200	2000	
V_{CC} Fall Time (Note 4)	t_F	Figure 5	10			µs
V_{CC} Rise Time (Note 4)	t_R	Figure 6	0			µs
V_{CC} Detect to RST High and RST Low	t_{RPD}	Figure 7, V_{CC} falling			100	ns
V_{CC} Detect to RST Low and RST Open (Note 6)	t_{RPU}	Figure 8, V_{CC} rising	250	610	1000	ms

Note 1: $\overline{PB\ RST}$ is internally pulled up to V_{CC} with an internal impedance of typically 40kΩ.
Note 2: Measured with outputs open.
Note 3: All voltages referenced to GND.
Note 4: Guaranteed by design.
Note 5: $\overline{PB\ RST}$ must be held low for a minimum of 20ms to guarantee a reset.
Note 6: t_R = 5µs.

Pin Description

NAME	FUNCTION
PB $\overline{RST}$	Pushbutton Reset Input. A debounced active-low input that ignores pulses less than 1ms in duration and is guaranteed to recognize inputs of 20ms or greater.
TD	Time Delay Set. The watchdog timebase select input (t_{TD} = 150ms for TD = 0V, t_{TD} = 600ms for TD = open, t_{TD} = 1.2sec for TD = V_{CC}).
TOL	Tolerance Input. Connect to GND for 5% tolerance or to V_{CC} for 10% tolerance.
GND	Ground
RST	Reset Output (Active High) - goes active: 1. If V_{CC} falls below the selected reset voltage threshold 2. If $\overline{PB\ RST}$ is forced low 3. If $\overline{ST}$ is not strobed within the minimum timeout period 4. During power-up
$\overline{RST}$	Reset Output (Active Low, Open Drain) - see RST.
ST	Strobe Input. Input for watchdog timer.
V_{CC}	The +5V Power-Supply Input
N.C.	No Connect

Detailed Description

Power Monitor

A voltage detector monitors V_{CC} and holds the reset outputs (RST and $\overline{RST}$) in their active states whenever V_{CC} is below the selected 5% or 10% tolerance (4.62V or 4.37V typically). To select the 5% level, connect TOL to ground. To select the 10% level, connect TOL to V_{CC}. The reset outputs will remain in their active states until V_{CC} has been continuously in-tolerance for a minimum of 250ms (the reset active time) to allow the power supply and µP to stabilize.

The RST output both sinks and sources current, while the $\overline{RST}$ output, an open-drain MOSFET, sinks current only and must be pulled high.

Pushbutton Reset Input

The MAX1232's debounced manual reset input ($\overline{PB\ RST}$) manually forces the reset outputs into their active states. The reset outputs go active after $\overline{PB\ RST}$ has been held low for a time t_{PBD}, the pushbutton reset delay time. The reset outputs remain in their active states for a minimum of 250ms after $\overline{PB\ RST}$ rises above V_{IH} (Figure 3).

A mechanical pushbutton or an active logic signal can drive the $\overline{PB\ RST}$ input. The debounced input ignores input pulses less than 1ms and is guaranteed to recognize pulses of 20ms or greater. The $\overline{PB\ RST}$ input has an internal pull-up to V_{CC} of about 100µA; therefore, an external pull-up resistor is not necessary.

Watchdog Timer

The µP drives the $\overline{ST}$ input with an Input/Output (I/O) line. The µP must toggle the $\overline{ST}$ input within a set period (as determined by TD) to verify proper software execution. If a hardware or software failure keeps $\overline{ST}$ from toggling within the minimum timeout period – ST is activated only by falling edges (a high-to-low transition) – the MAX1232 reset outputs are forced to their active states for 250ms (Figure 2). This typically initiates the µP's power-up routine. If the interruption continues, new reset pulses are generated each timeout period until $\overline{ST}$ is strobed. The timeout period is determined by the TD input connection. This timeout period is typically 150ms with TD connected to GND, 600ms with TD floating, or 1200ms with TD connected to V_{CC}.

The software routine that strobes $\overline{ST}$ is critical. The code must be in a section of software that executes frequently enough so the time between toggles is less than the watchdog timeout period. One common technique controls the µP I/O line from two sections of the program. The software might set the I/O line high while operating in the foreground mode and set it low while in the background or interrupt mode. If both modes do not execute correctly, the watchdog timer issues reset pulses.

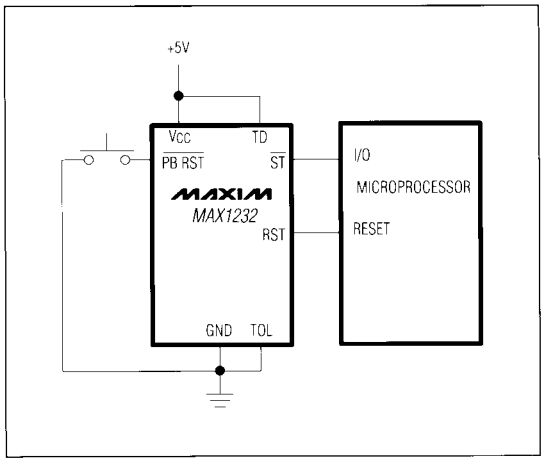


Figure 1. Pushbutton Reset

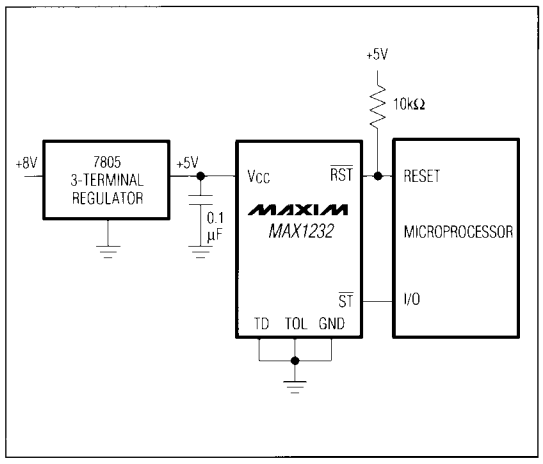
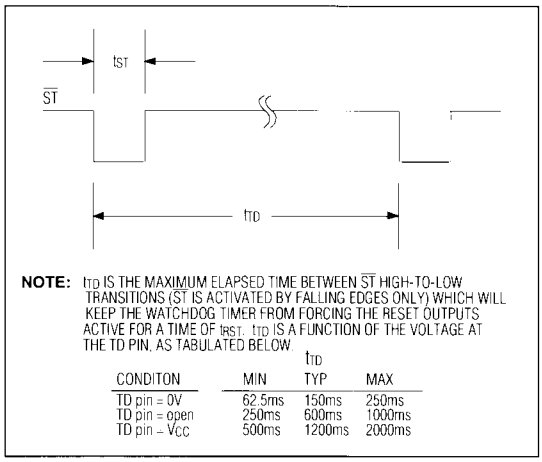


Figure 2. Watchdog Timer



NOTE: t_{TD} IS THE MAXIMUM ELAPSED TIME BETWEEN $\overline{ST}$ HIGH-TO-LOW TRANSITIONS ($\overline{ST}$ IS ACTIVATED BY FALLING EDGES ONLY) WHICH WILL KEEP THE WATCHDOG TIMER FROM FORCING THE RESET OUTPUTS ACTIVE FOR A TIME OF t_{RST}. t_{TD} IS A FUNCTION OF THE VOLTAGE AT THE TD PIN, AS TABULATED BELOW.

	t_{TD}		
CONDITON	MIN	TYP	MAX
TD pin = 0V	62.5ms	150ms	250ms
TD pin = open	250ms	600ms	1000ms
TD pin = V_{CC}	500ms	1200ms	2000ms

Figure 4. Watchdog Strobe Input

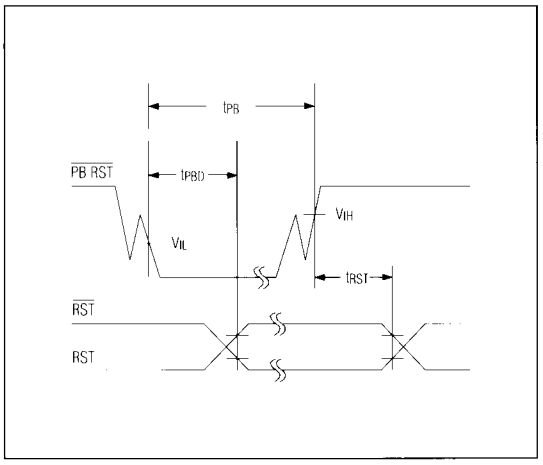


Figure 3. Pushbutton Reset. The debounced $\overline{PB\ RST}$ input ignores input pulses less than 1ms and is guaranteed to recognize pulses of 20ms or greater.

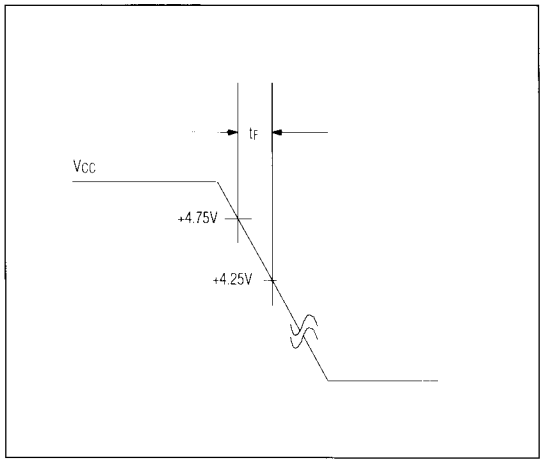


Figure 5. Power-Down Slew Rate

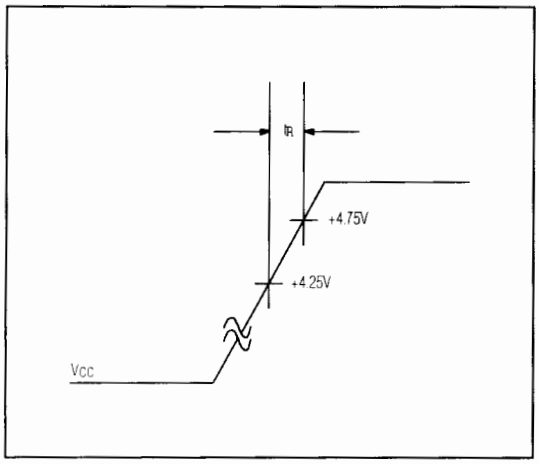


Figure 6. Power-Up Slew Rate

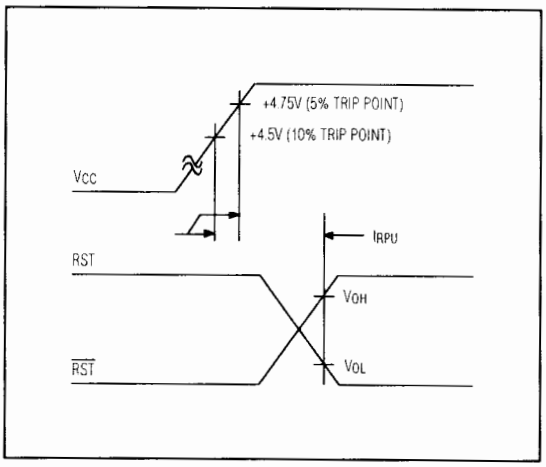


Figure 8. VCC Detect Reset Output Delay (Power-Up)

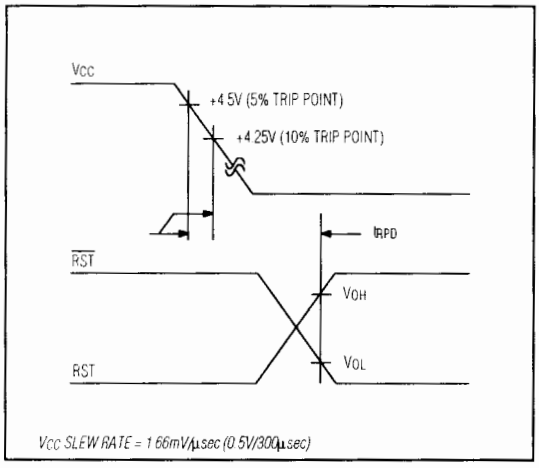


Figure 7. VCC Detect Reset Output Delay (Power-Down)

Chip Topography