

Order code	Manufacturer code	Description
83-0880	n/a	74HC259D 8-BIT ADDRESSABLE LATCH SO16 RC

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The enclosed information is believed to be correct, Information may change without notice due to product improvement. Users should ensure that the product is suitable for their use. E. & O. E.	Revision A 20/02/2007

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT259** 8-bit addressable latch

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-bit addressable latch

## 74HC/HCT259

## FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT259 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT259 are high-speed 8-bit addressable latches designed for general purpose storage applications in digital systems. The "259" are multifunctional devices

capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q<sub>0</sub> to Q<sub>7</sub>), functions are available.

The "259" also incorporates an active LOW common reset ( $\overline{\text{MR}}$ ) for resetting all latches, as well as, an active LOW enable input ( $\overline{\text{LE}}$ ).

The "259" has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A<sub>0</sub> to A<sub>2</sub>) and data (D) input. When operating the "259" as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the "259".

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D to Q <sub>n</sub> A <sub>n</sub> , $\overline{\text{LE}}$ to Q <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	18	20	ns
	A <sub>n</sub> , $\overline{\text{LE}}$ to Q <sub>n</sub>		17	20	ns
t <sub>PHL</sub>	$\overline{\text{MR}}$ to Q <sub>n</sub>		15	20	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

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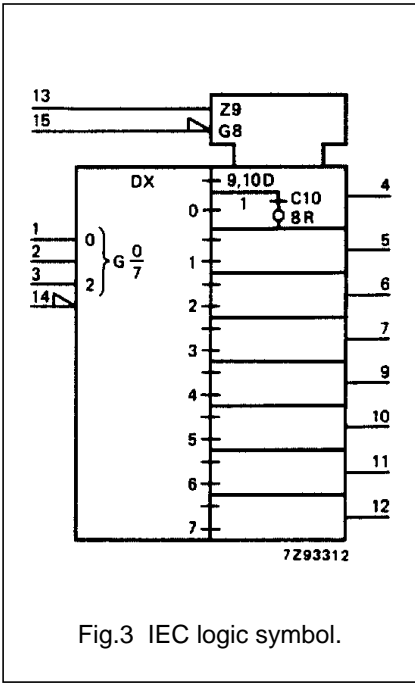
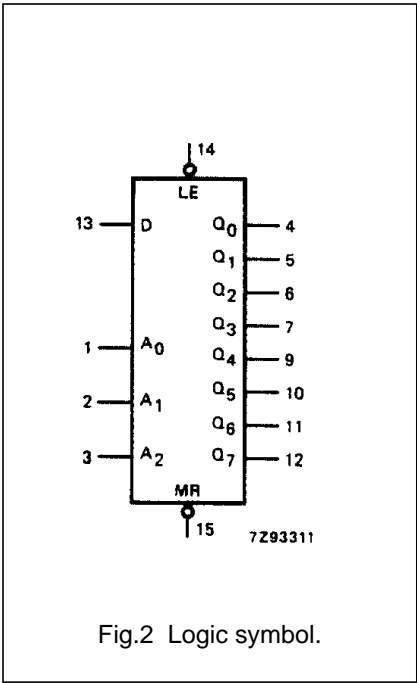
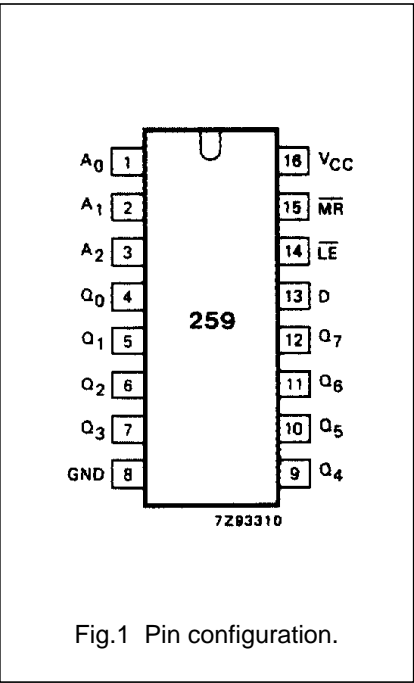
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ORDERING INFORMATION

See “74HC/HCT/HCU/HCMOS Logic Package Information”.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A <sub>0</sub> to A <sub>2</sub>	address inputs
4, 5, 6, 7, 9 10, 11, 12	Q <sub>0</sub> to Q <sub>7</sub>	latch outputs
8	GND	ground (0 V)
13	D	data input
14	$\overline{\text{LE}}$	latch enable input (active LOW)
15	$\overline{\text{MR}}$	conditional reset input (active LOW)
16	V <sub>CC</sub>	positive supply voltage



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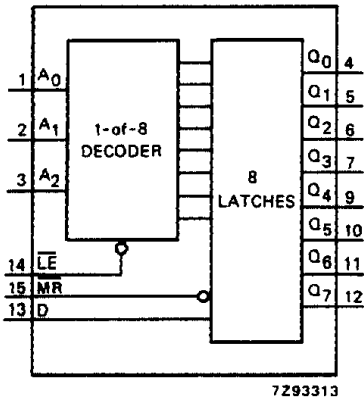


Fig.4 Functional diagram.

MODE SELECT TABLE

$\overline{LE}$	$\overline{MR}$	MODE
L	H	addressable latch
H	H	memory
L	L	active HIGH 8-channel demultiplexer
H	L	reset

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FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS							
	$\overline{\text{MR}}$	$\overline{\text{LE}}$	D	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>
master reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
store (do nothing)	H	H	X	X	X	X	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
addressable latch	H	L	d	L	L	L	Q=d	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	H	L	L	q <sub>0</sub>	Q=d	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	L	H	L	q <sub>0</sub>	q <sub>1</sub>	Q=d	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	H	H	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	Q=d	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	L	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	Q=d	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	H	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	Q=d	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	L	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	Q=d	q <sub>7</sub>
	H	L	d	H	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	Q=d

## Notes

1. H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH  $\overline{\text{LE}}$  transition  
q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared

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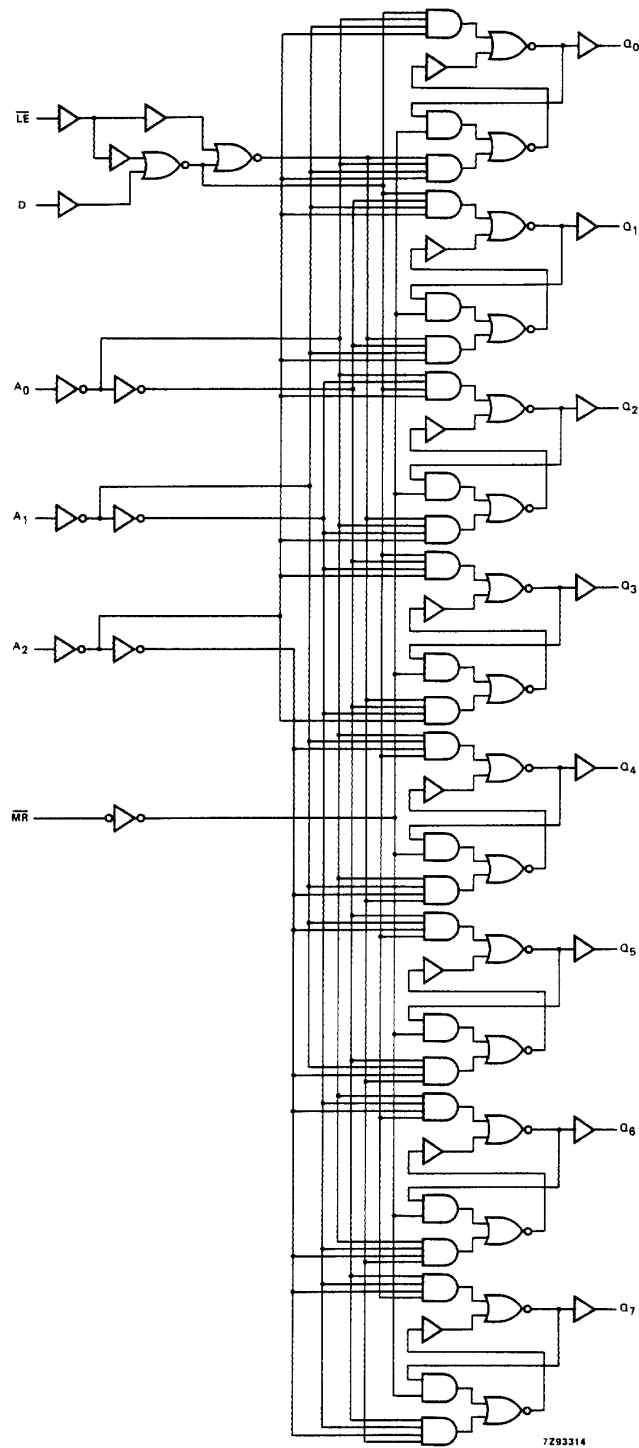


Fig.5 Logic diagram.

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D to Q <sub>n</sub>		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Q <sub>n</sub>		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{\text{LE}}$ to Q <sub>n</sub>		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		119 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
t <sub>W</sub>	$\overline{\text{LE}}$ pulse width HIGH or LOW	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	$\overline{\text{MR}}$ pulse width LOW	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig.9
t <sub>su</sub>	set-up time D, A <sub>n</sub> to $\overline{\text{LE}}$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 10 and 11
t <sub>h</sub>	hold time D to $\overline{\text{LE}}$	0 0 0	−19 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.10
t <sub>h</sub>	hold time A <sub>n</sub> to $\overline{\text{LE}}$	2 2 2	−11 −4 −3		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.11



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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{A_n}$	1.50
$\overline{LE}$	1.50
$\overline{D}$	1.20
$\overline{MR}$	0.75

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**AC CHARACTERISTICS FOR 74HCT**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 TO +85		−40 TO +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D to Q <sub>n</sub>		23	39		49		59	ns	4.5	Fig.7	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Q <sub>n</sub>		25	41		51		62	ns	4.5	Fig.8	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		22	38		48		57	ns	4.5	Fig.6	
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		23	39		49		59	ns	4.5	Fig.9	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	
t <sub>W</sub>	LE pulse width LOW	19	11		24		29		ns	4.5	Fig.6	
t <sub>W</sub>	MR pulse width LOW	18	10		23		27		ns	4.5	Fig.9	
t <sub>su</sub>	set-up time D to LE	17	10		21		26		ns	4.5	Fig.10	
t <sub>su</sub>	set-up time A <sub>n</sub> to LE	17	10		21		26		ns	4.5	Fig.11	
t <sub>h</sub>	hold time D to LE	0	−8		0		0		ns	4.5	Fig.10	
t <sub>h</sub>	hold time A <sub>n</sub> to LE	0	−4		0		0		ns	4.5	Fig.11	

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## AC WAVEFORMS

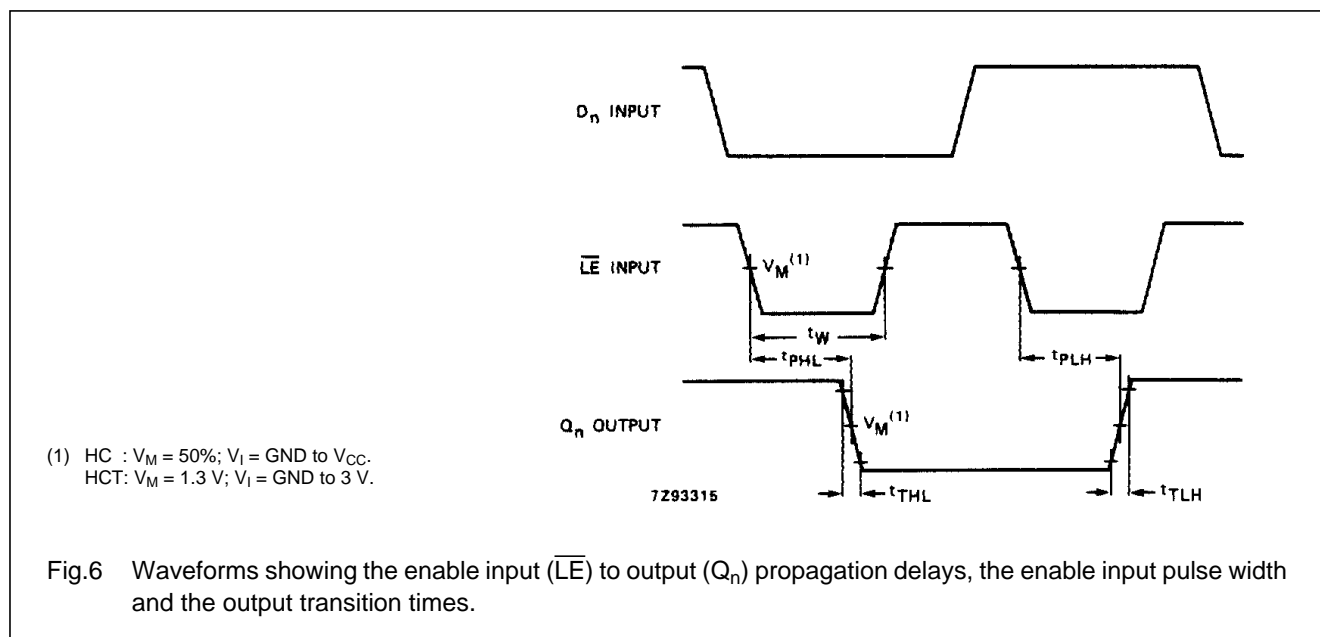


Fig.6 Waveforms showing the enable input ( $\overline{LE}$ ) to output ( $Q_n$ ) propagation delays, the enable input pulse width and the output transition times.

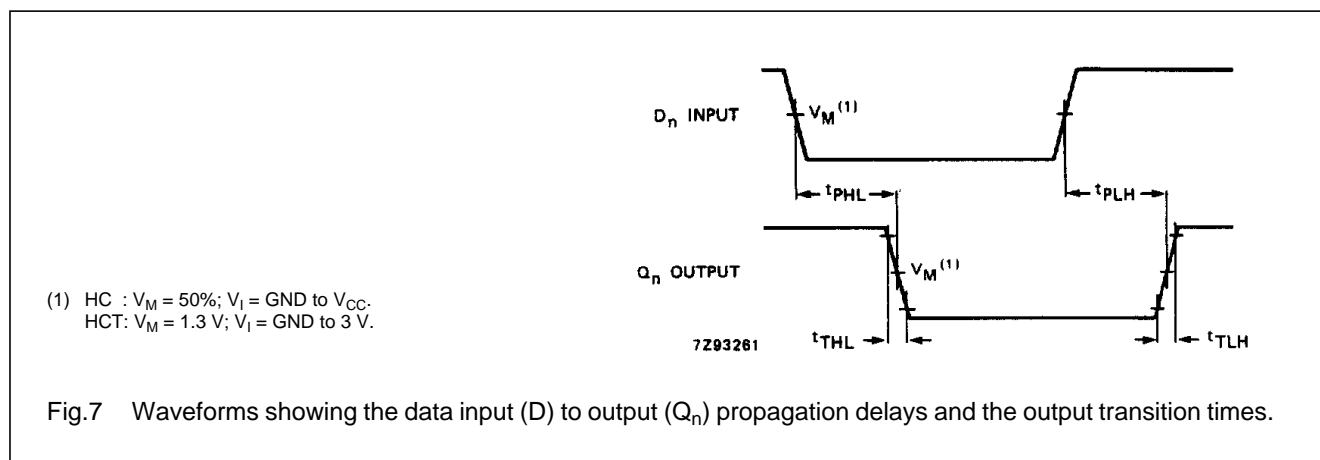


Fig.7 Waveforms showing the data input ( $D$ ) to output ( $Q_n$ ) propagation delays and the output transition times.

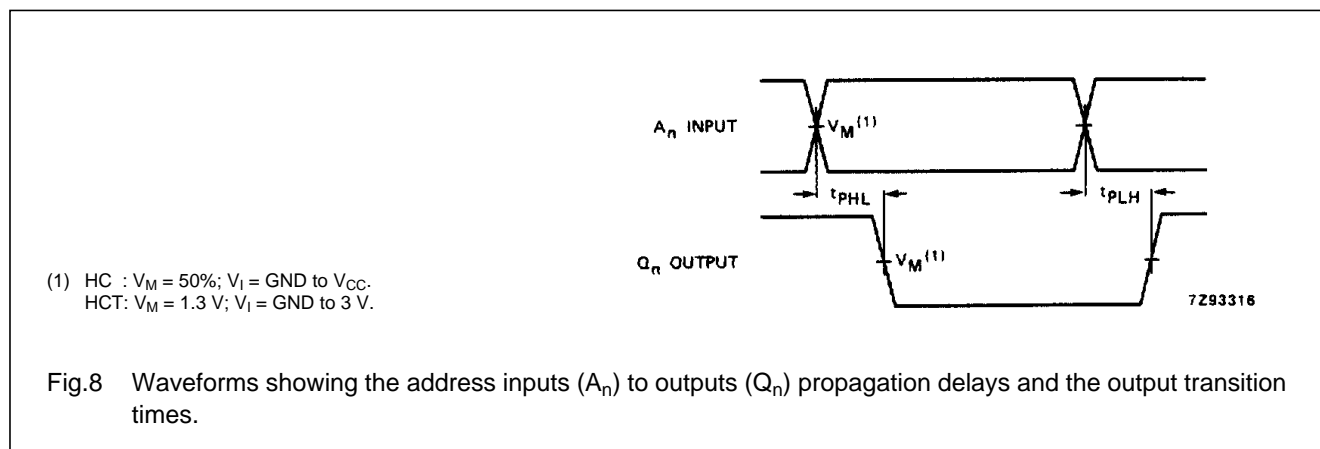
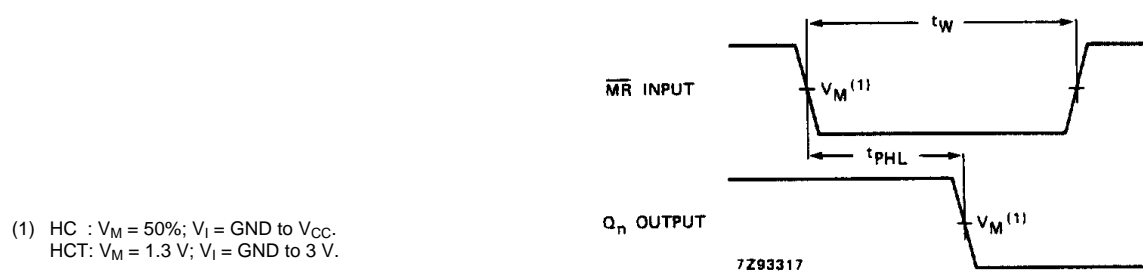
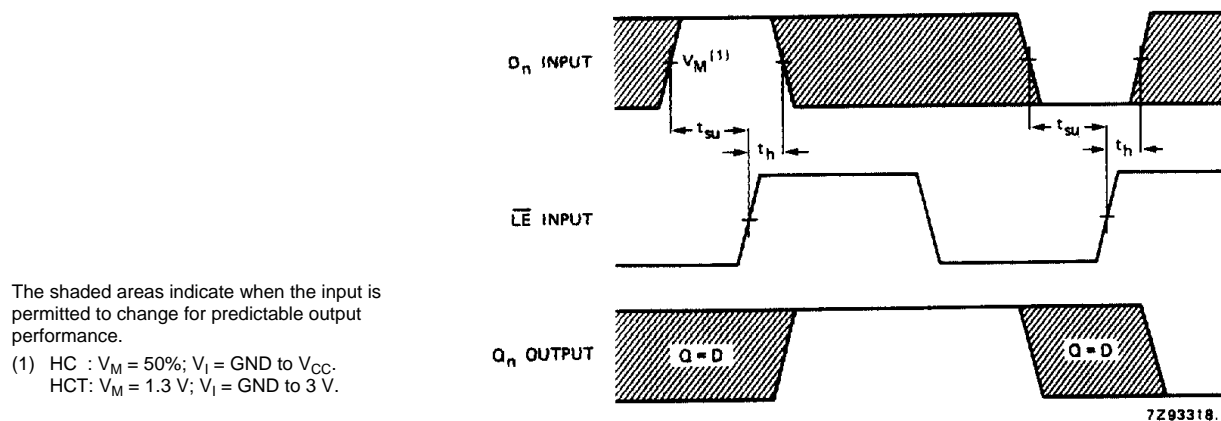
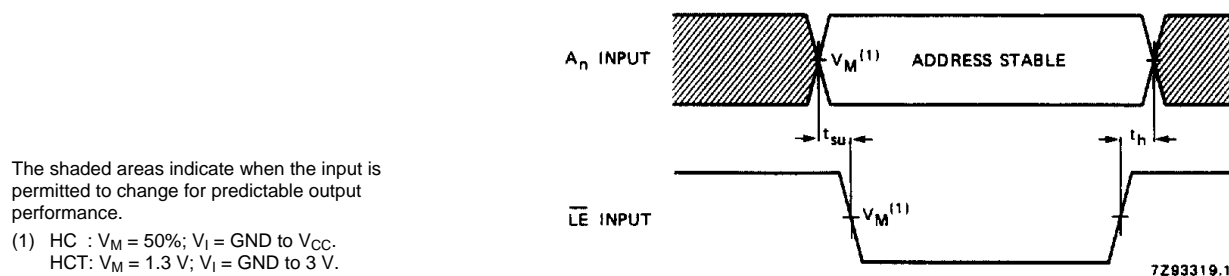


Fig.8 Waveforms showing the address inputs ( $A_n$ ) to outputs ( $Q_n$ ) propagation delays and the output transition times.

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Fig.9 Waveforms showing the conditional reset input ( $\overline{\text{MR}}$ ) to output ( $Q_n$ ) propagation delays.Fig.10 Waveforms showing the data set-up and hold times for the D input to  $\overline{\text{LE}}$  input.Fig.11 Waveforms showing the address set-up and hold times for  $A_n$  inputs to  $\overline{\text{LE}}$  input.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".